

P2005 A01	
2GB GDDR5, 256b, 64Mx32	
Stacked DVI -I /DVI -D + HDMI + DP	
TABLE OF CONTENTS	
Page	Descripti on
1	Table of Contents
2	Block Diagram
3	PCI Express
4	MEMORY: GPU Partit ion A/B
5	MEMORY: FBA[31:0]
6	MEMORY: FBA[63:32]
7	MEMORY: FBB[31:0]
8	MEMORY: FBB[63:32]
9	MEMORY: GPU Partit ion C/D
10	MEMORY: FBC[31:0]
11	MEMORY: FBC[63:32]
12	MEMORY: FBD[31:0]
13	MEMORY: FBD[63:32]
14	GPU PWR and GND
15	GPU Decoupling
16	DACA Interface
17	I FPAB DVI -I -DL
18	I FPEF DVI -D-DL
19	I FPC HDMI /DP
20	I FPD DP
21	MIOA/B Interface And Frame Lock
22	MISC1: Fan, Thermal, JTAG, GPIO, Stereo
23	MISC2: ROM, XTAL, Straps
24	PS: 5V, PEX_VDD
25	PS: FBVDD/Q
26	PS: NVVDD Controller
27	PS: NVVDD Phase 1, 3
28	PS: NVVDD Phase 2, 5
29	PS: NVVDD Phase 4
30	PS: Inputs, Filtering, and Monitoring
31	PS: Shutdown
32	PS: 12V Current Steering PSI Control and LED
33	MECH: Bracket/Thermal

ASSEMBLY

PAGE DETAIL

BASE LEVEL GENERIC SCHEMATIC ONLY

Table of Contents

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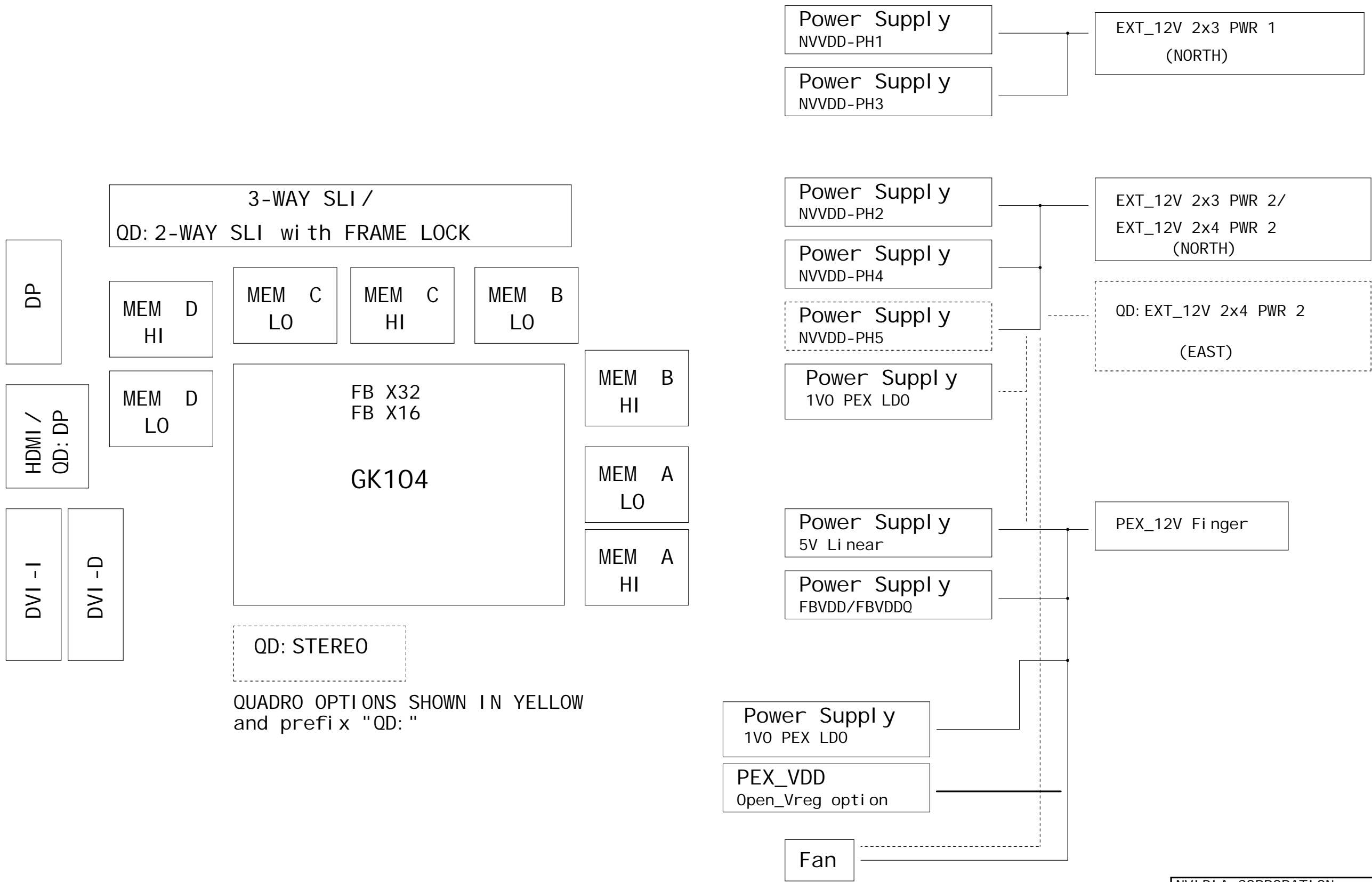
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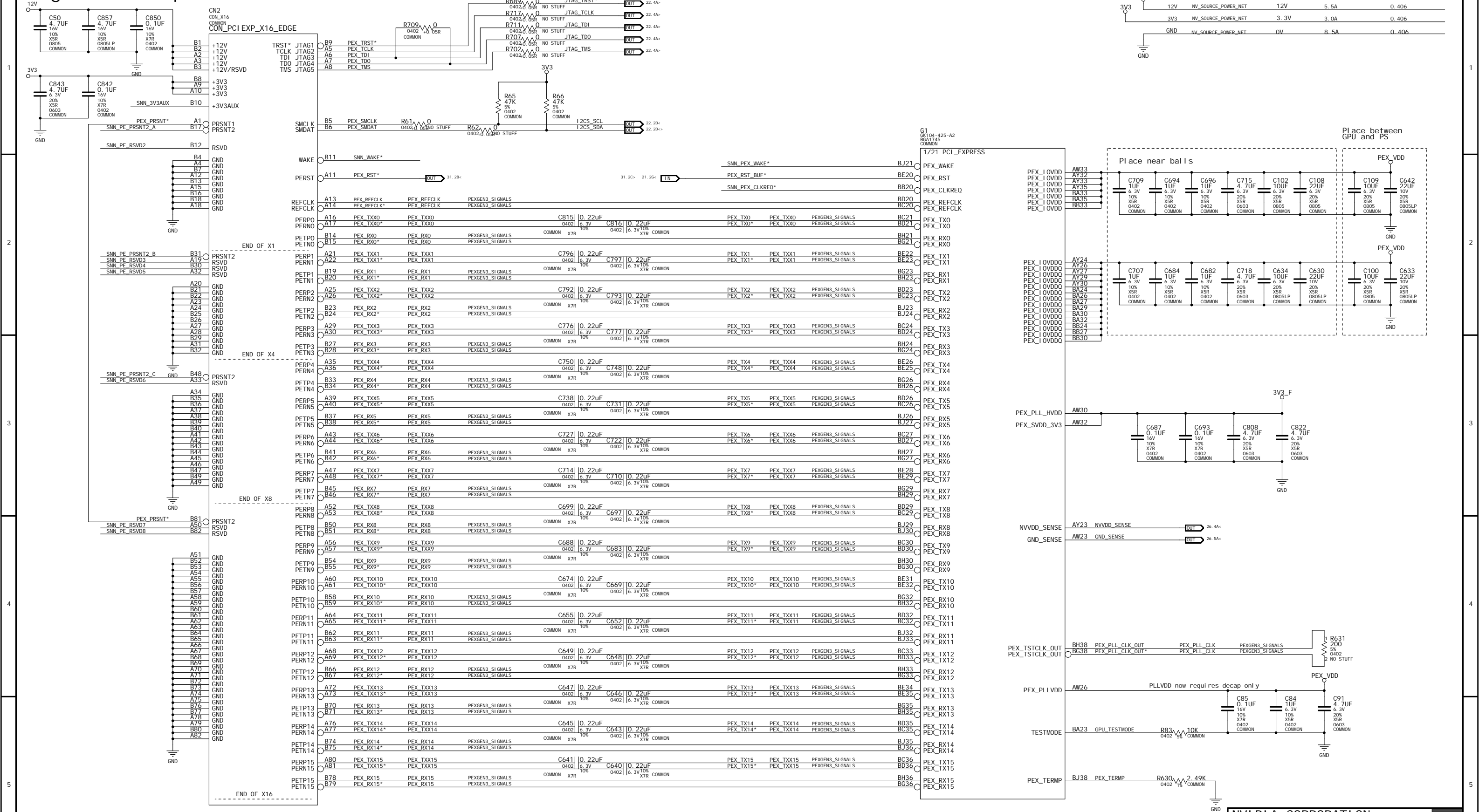
1 OF 33


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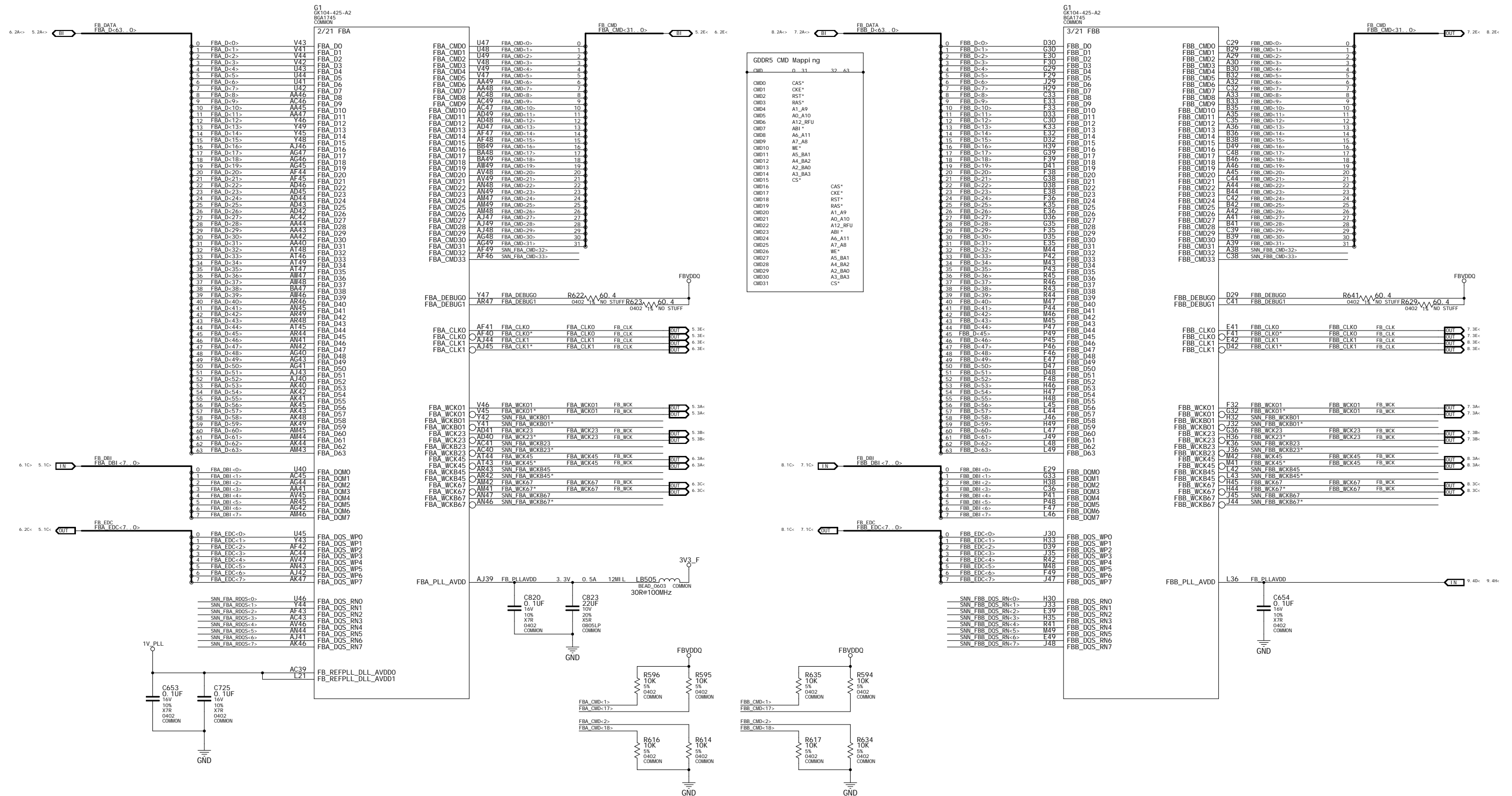
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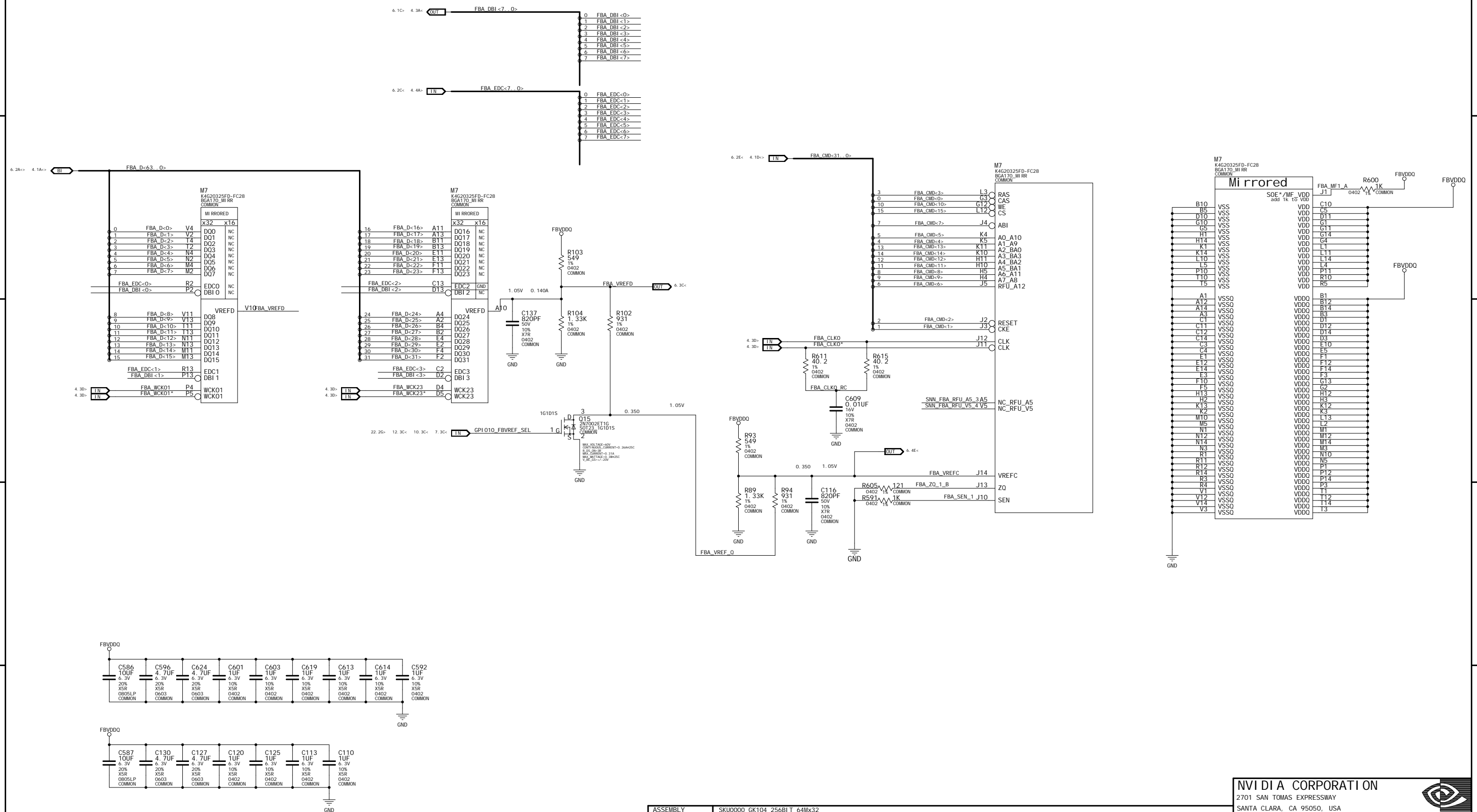


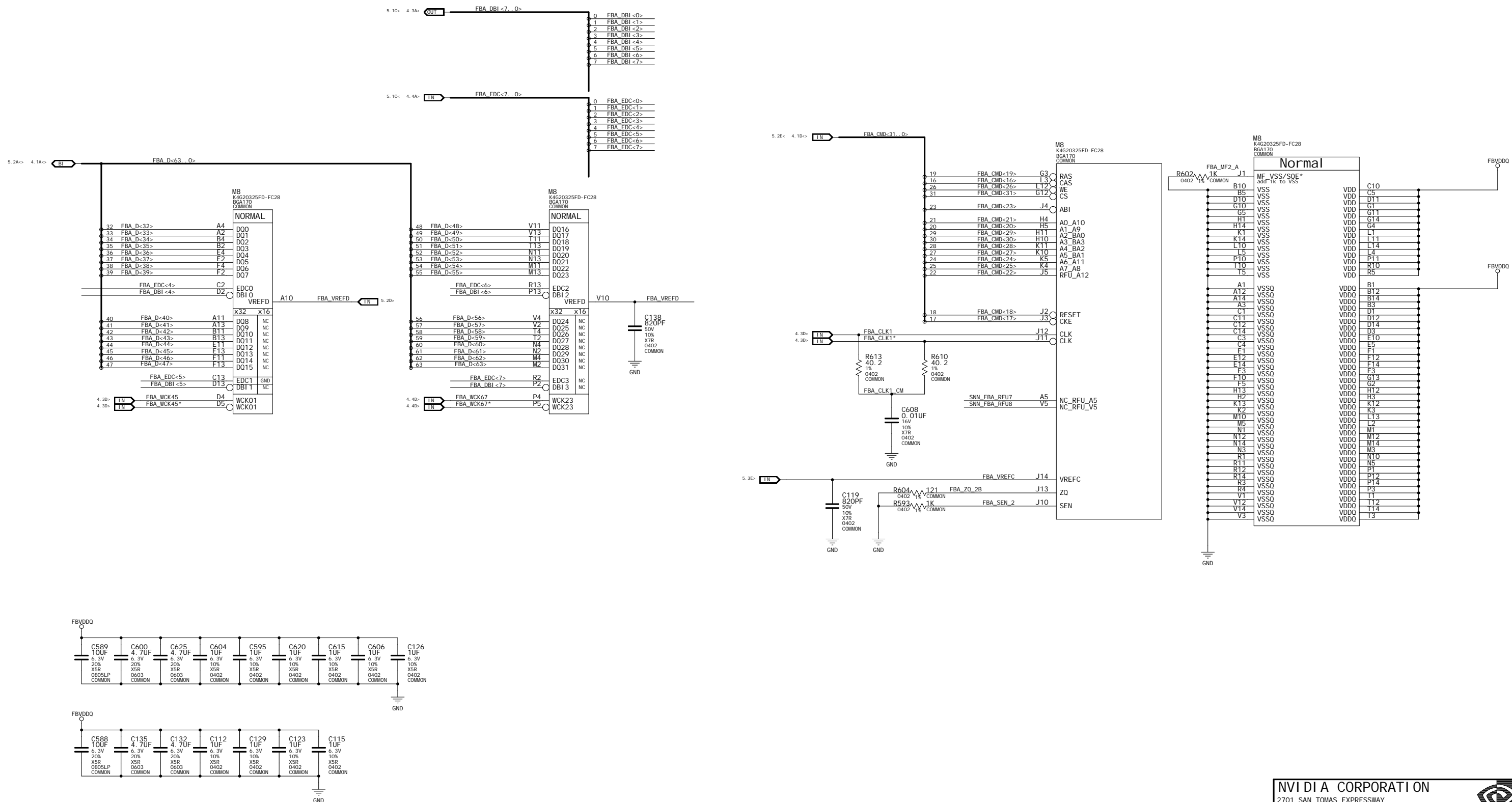
Page3: PCI Express

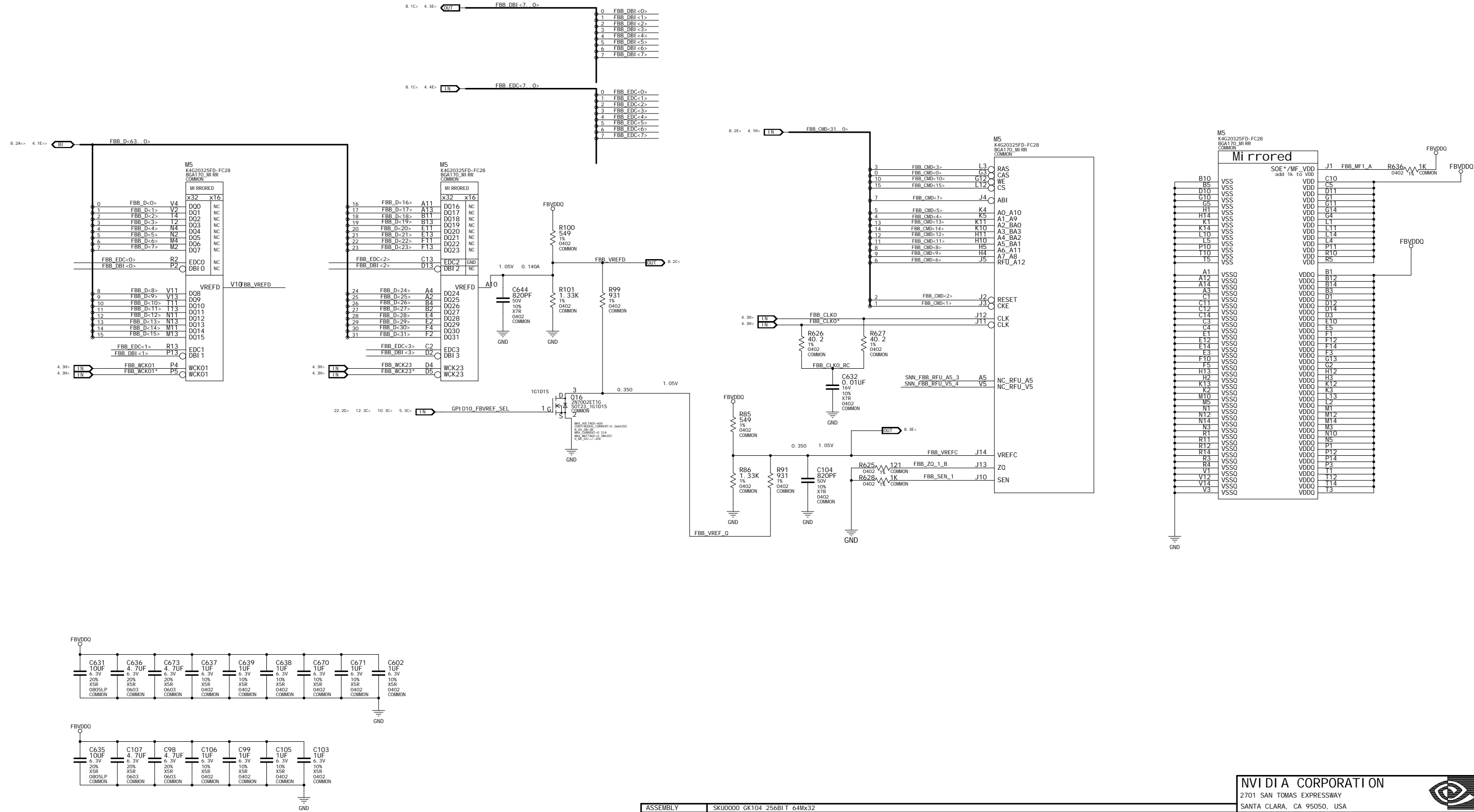


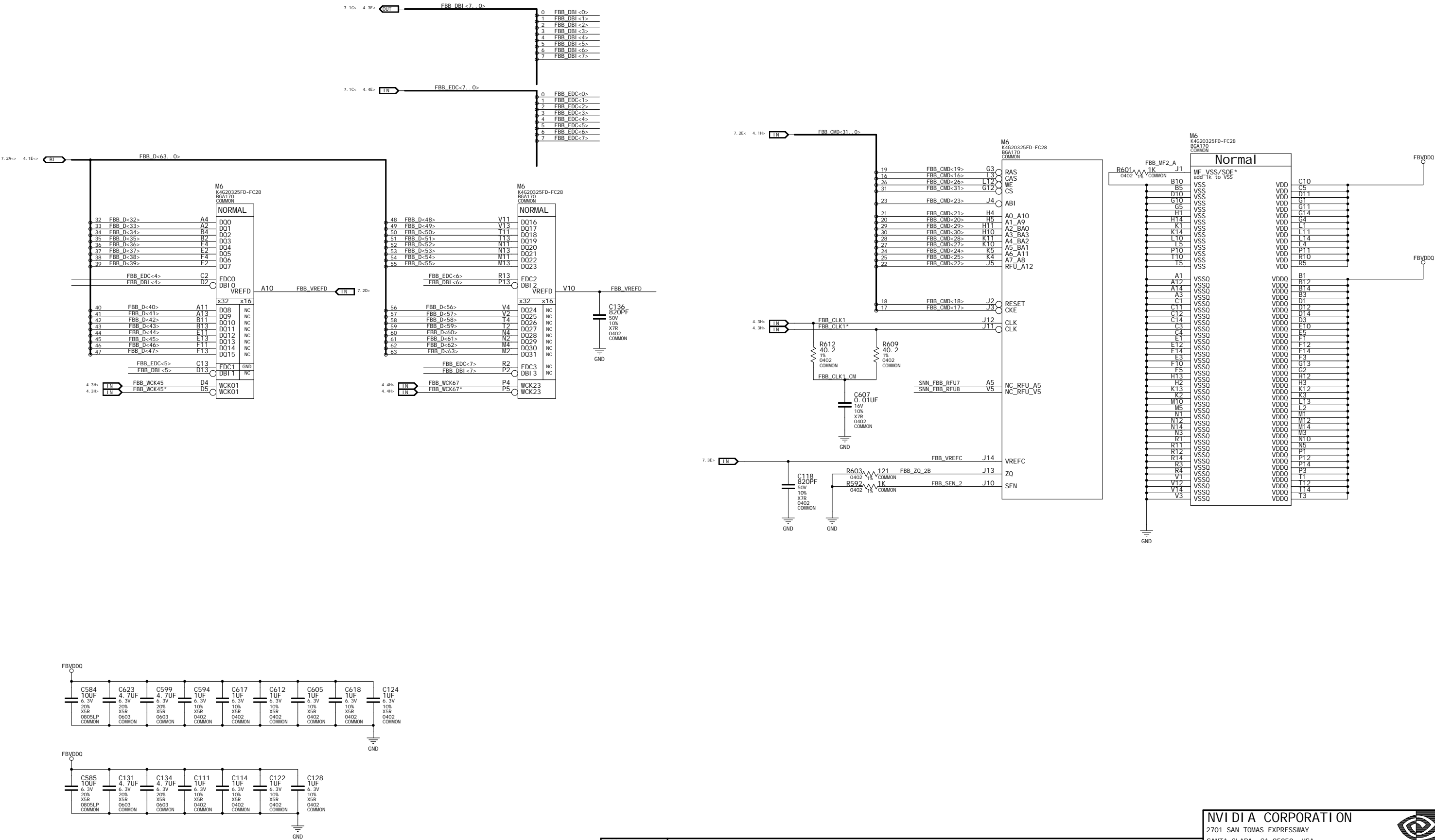
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PCB REV	P2005-A01	PAGE	3 OF 33
BOM REV	B	DATE	26-MAR-2013



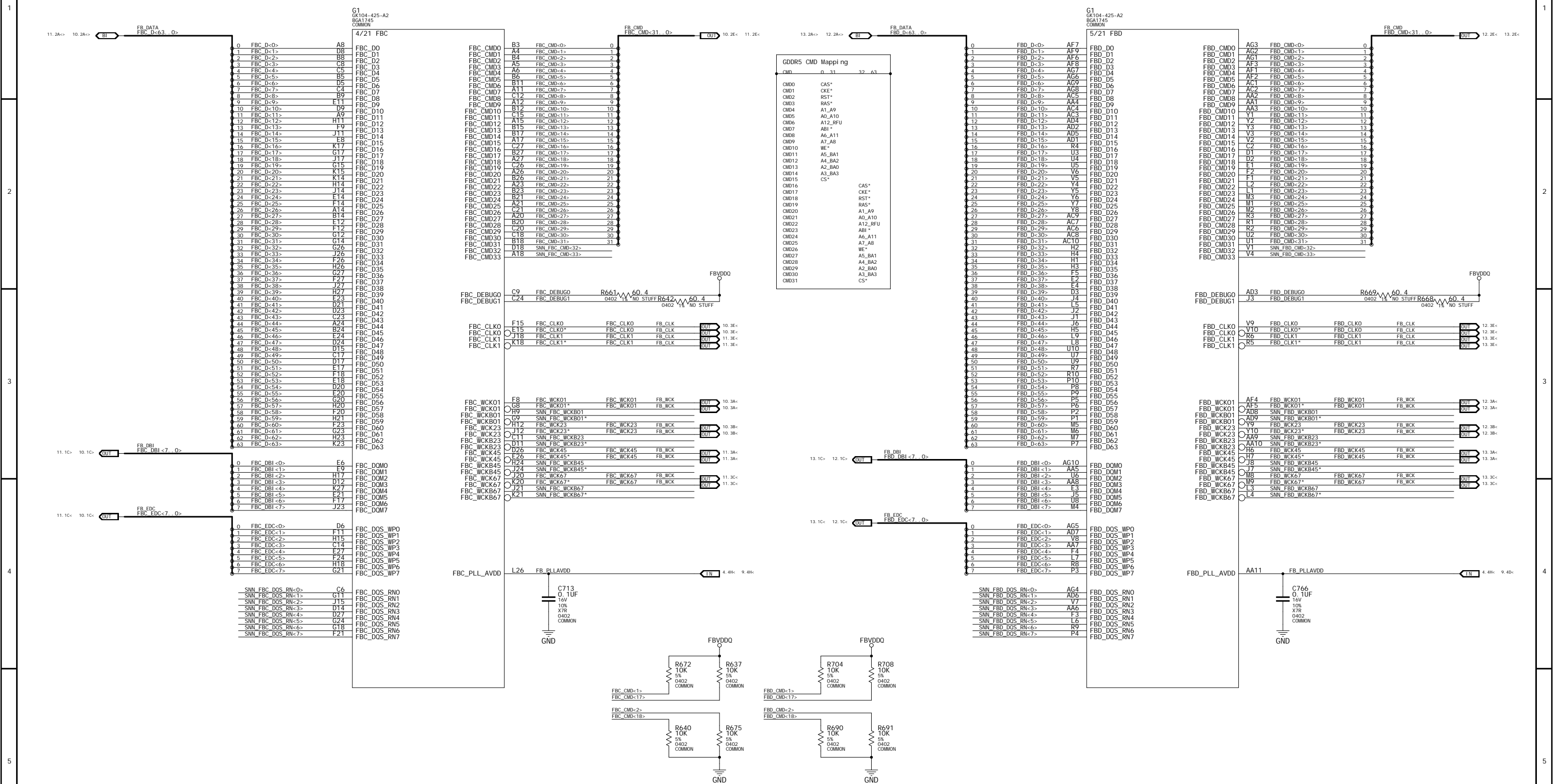


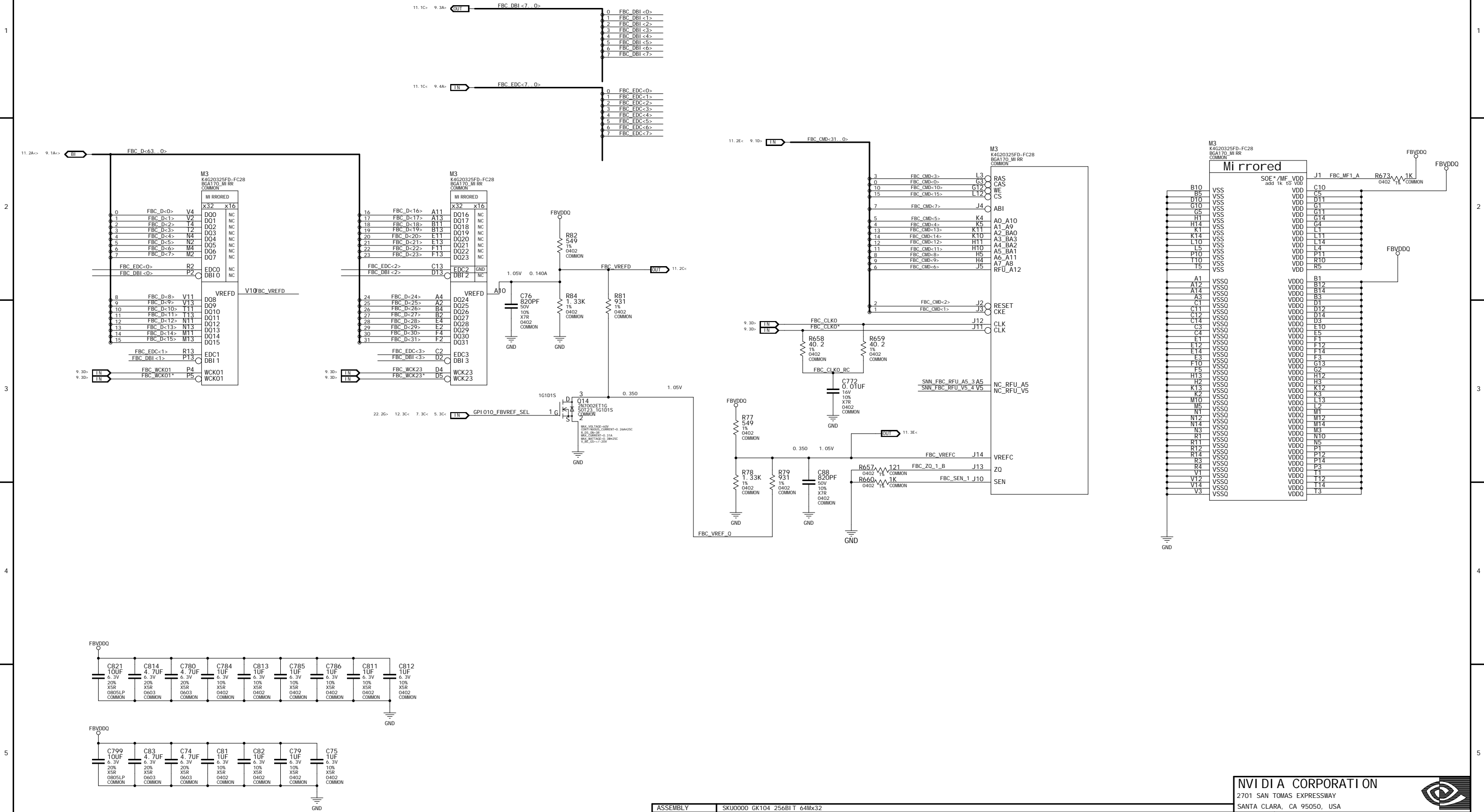




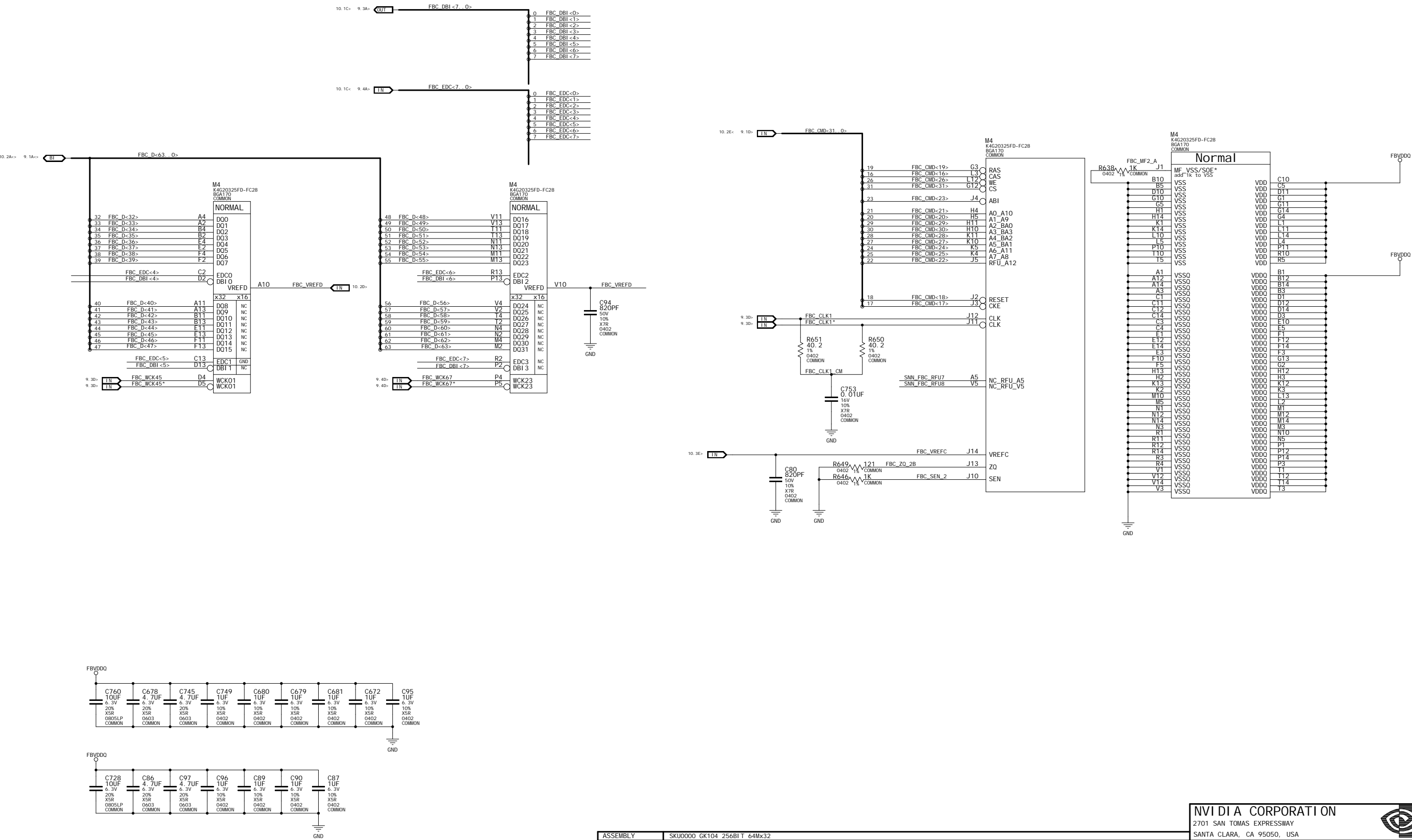


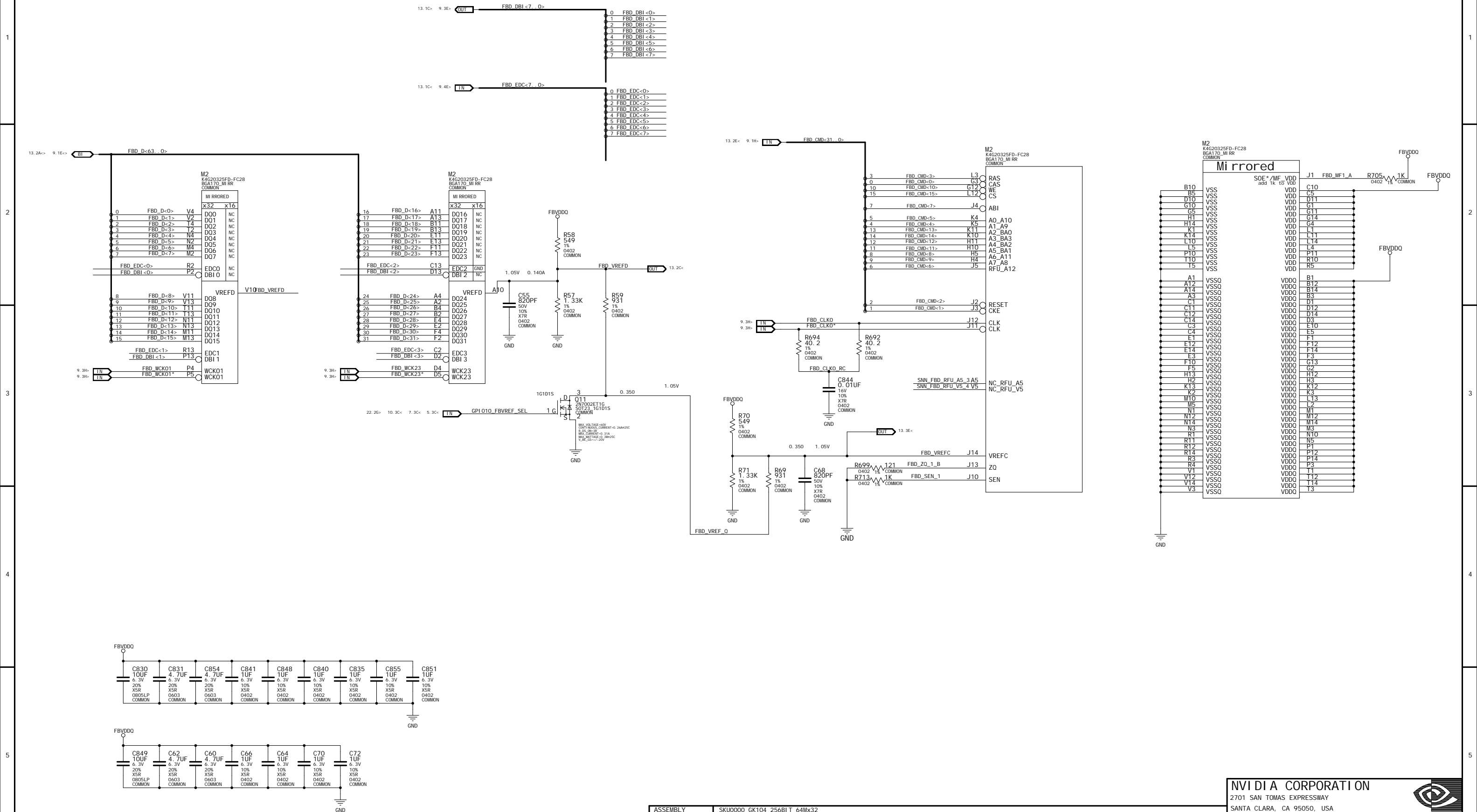
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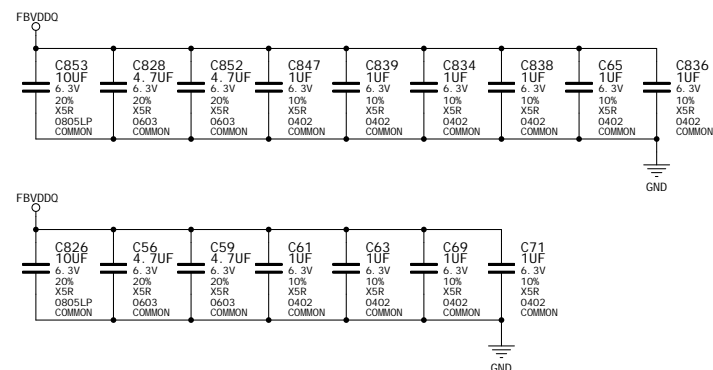
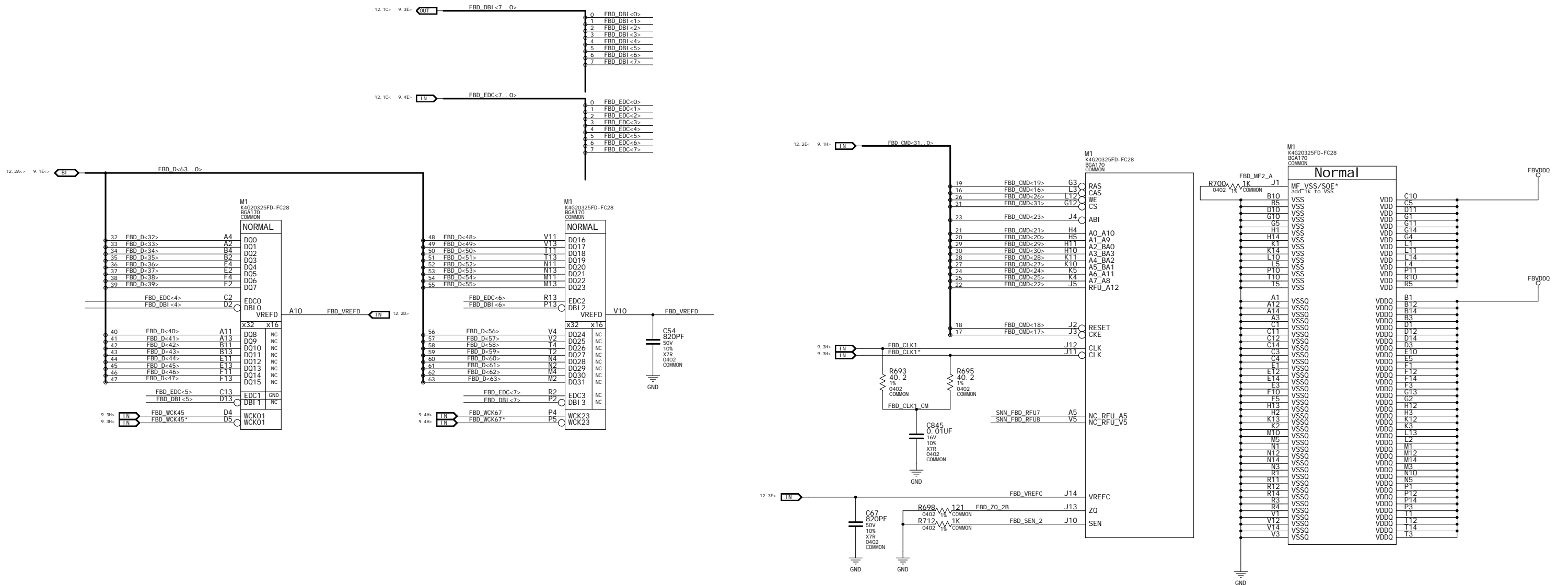


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Page13: MEMORY: FBD Parti ti on 63..32

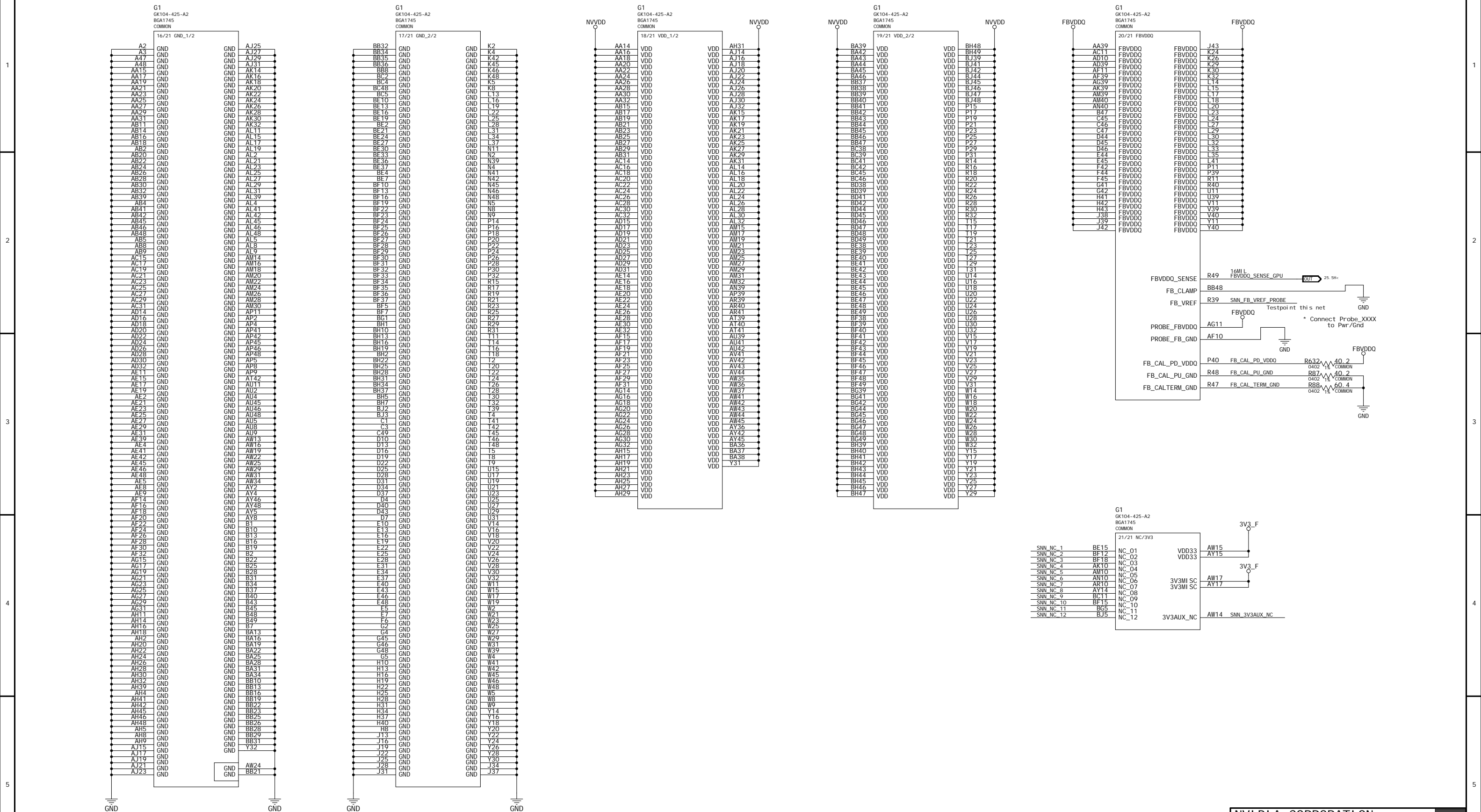


ASSEMBLY	SKU0000 GK104 256BIT 64Mx32
PAGE DETAIL	MEMORY: FBD[63: 32]

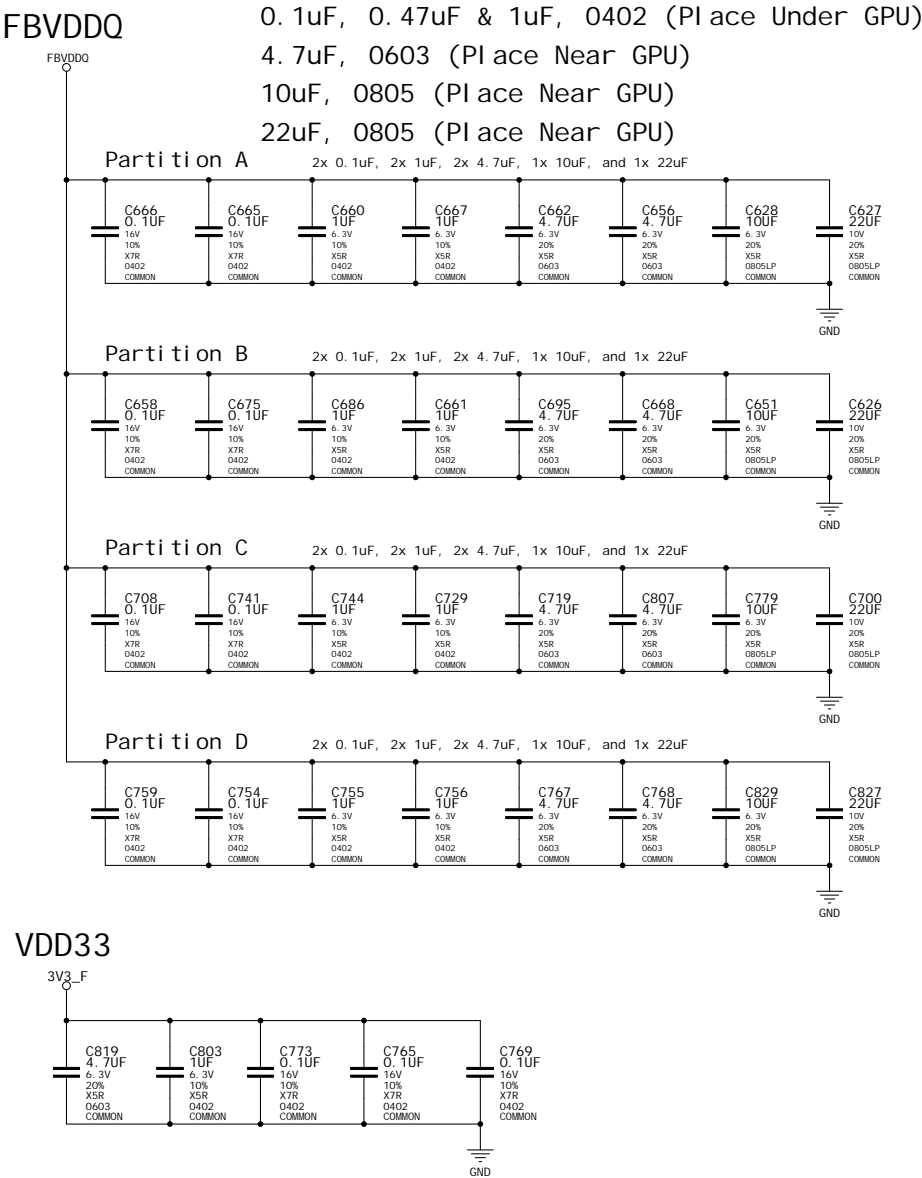
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PCB REV	P2005-A01	PAGE	13 OF 33
BOM REV	B	DATE	26-MAR-2013

Page14: GPU PWR and GND

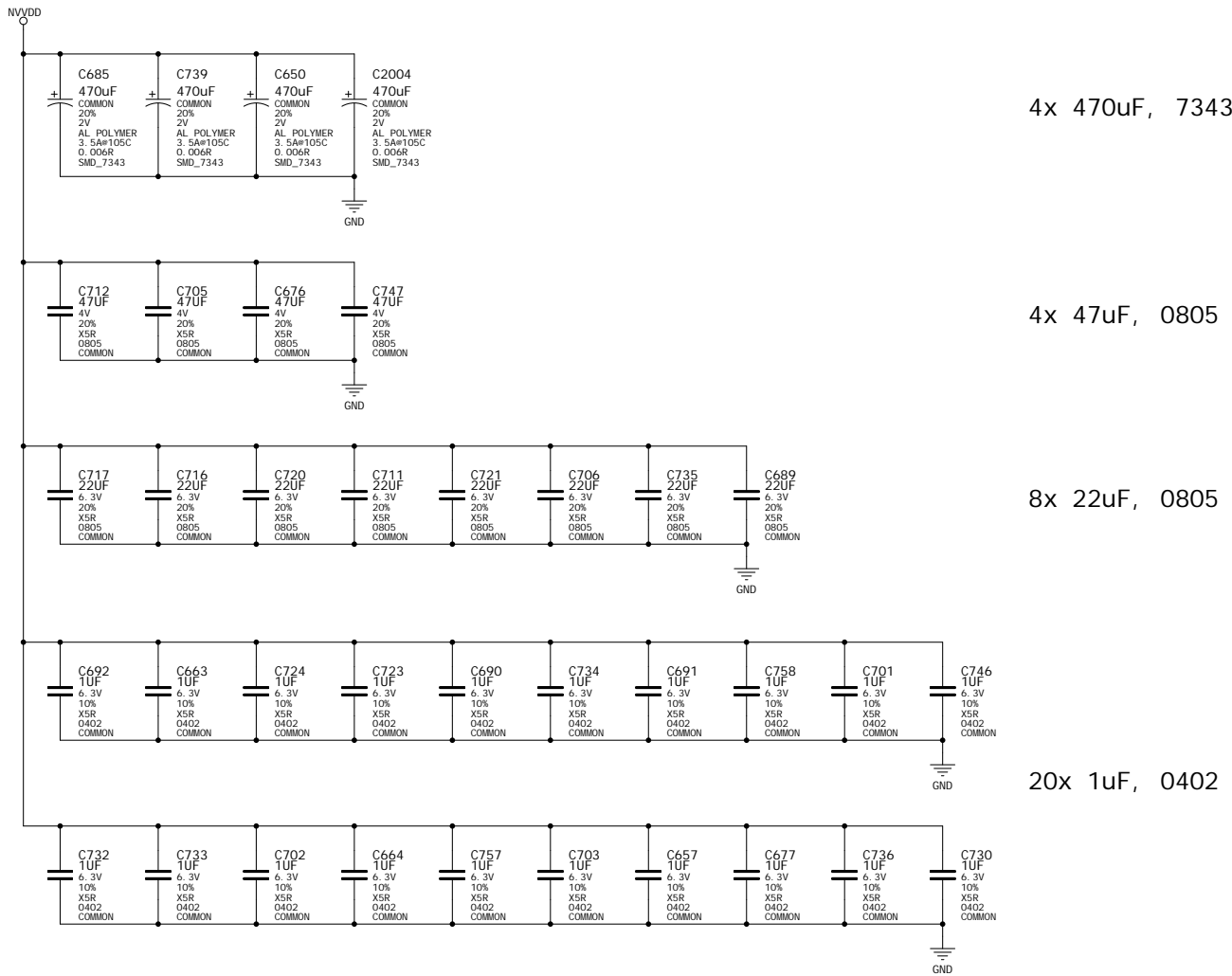


Based on GB2-X GDDR5 FBVDDQ Decap Guidel ine

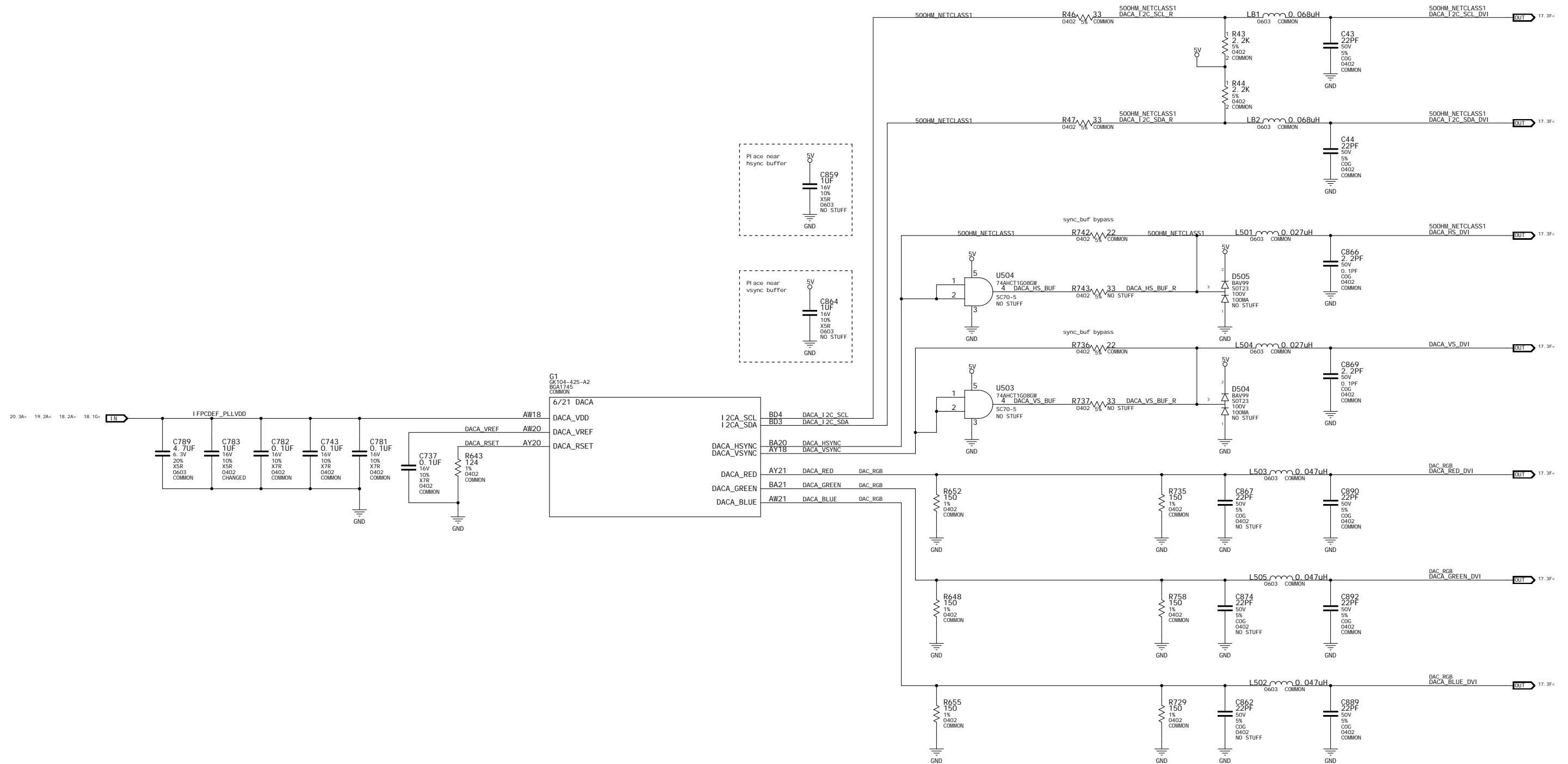


NVVDD Decoupl ing caps. Pl ace under GPU.

NVVDD



Page16: DACA Interface



ASSEMBLY	SKU0000 GK104 256BIT 64Mx32
PAGE DETAIL	DACA Interface

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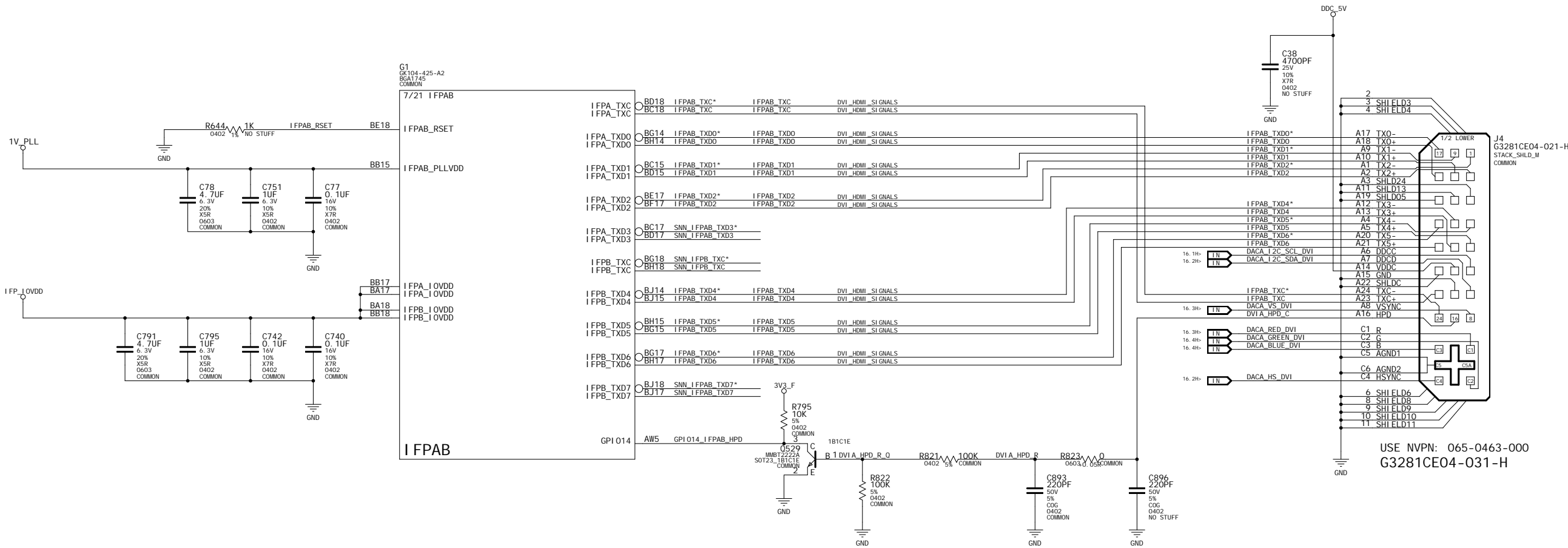
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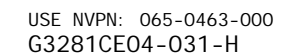
PCB REV	P2005-A01	PAGE	16 OF 33
BOM REV	B	DATE	26-MAR-2013

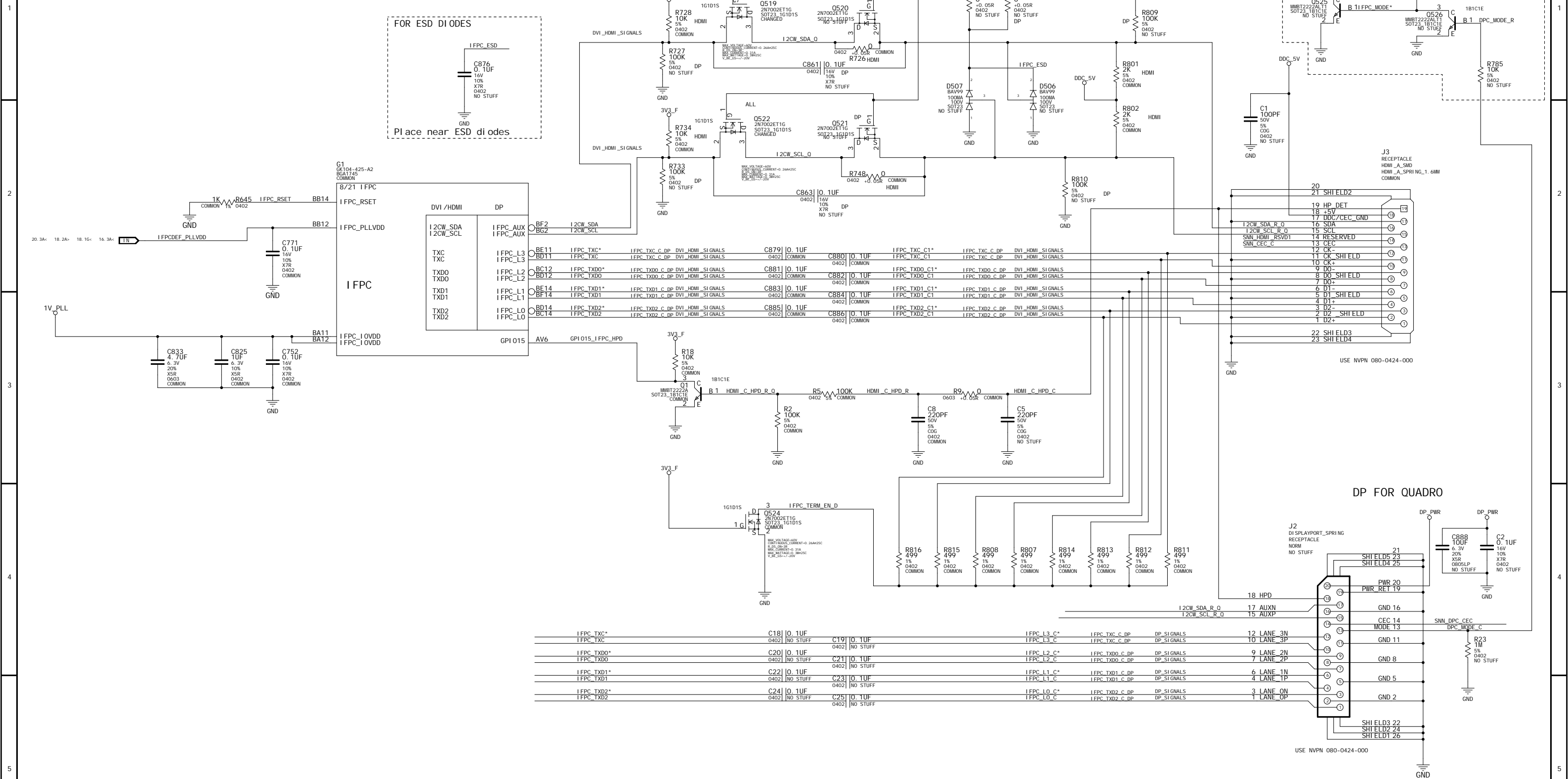


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PCB REV	P2005-A01	PAGE	17 OF 33
BOM REV	B	DATE	26-MAR-2013


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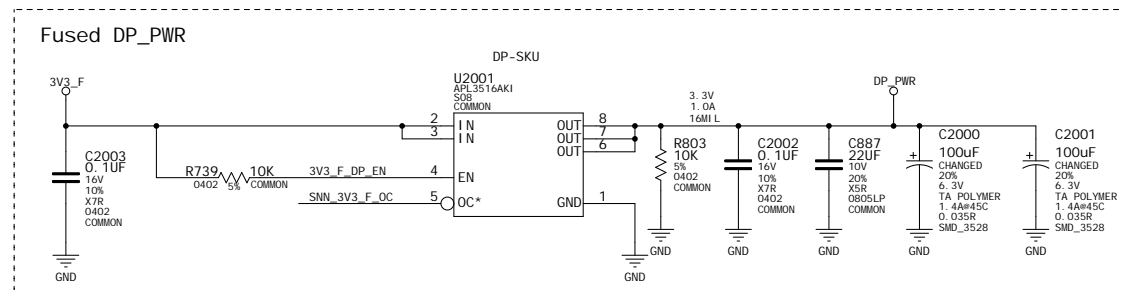
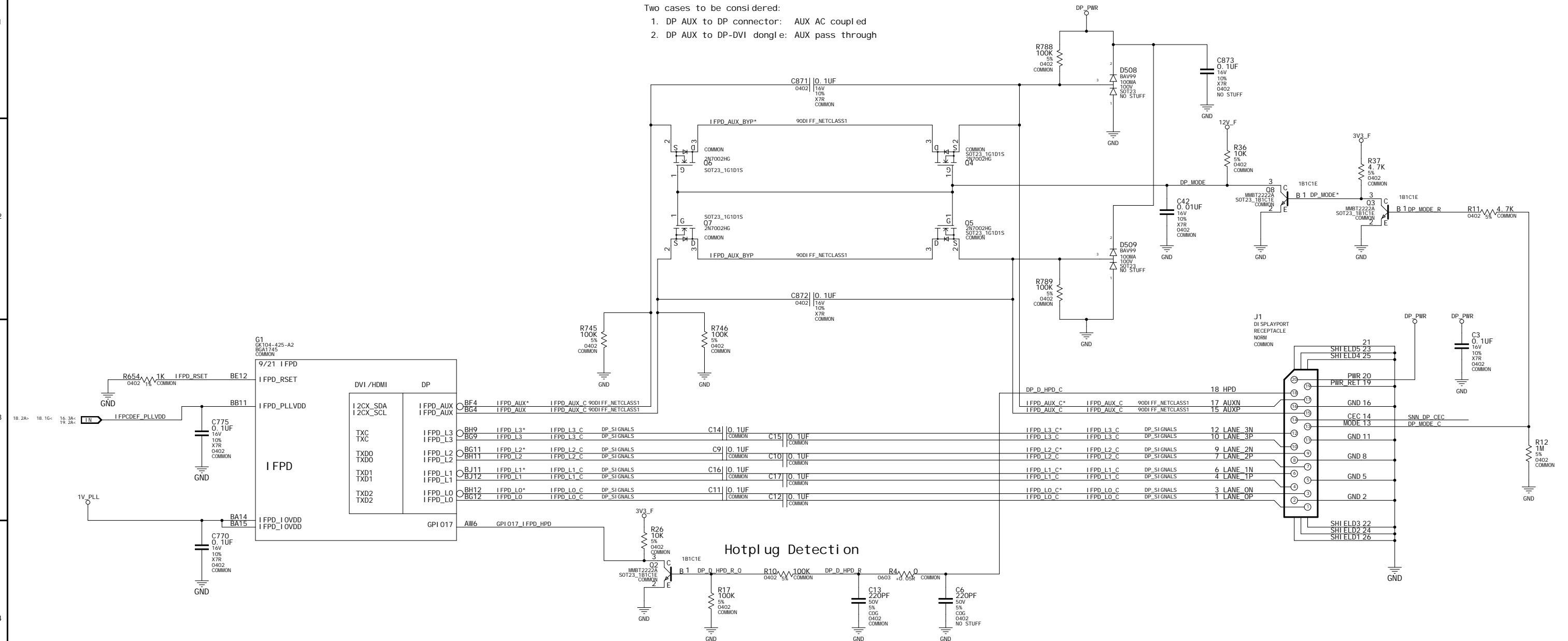
ASSEMBLY	SKU0000 GK104 256BIT 64Mx32
PAGE DETAIL	1 FPC HDMI /DP

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PCB REV	P2005-A01	PAGE	19 OF 33
BOM REV	B	DATE	26-MAR-2013


Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through

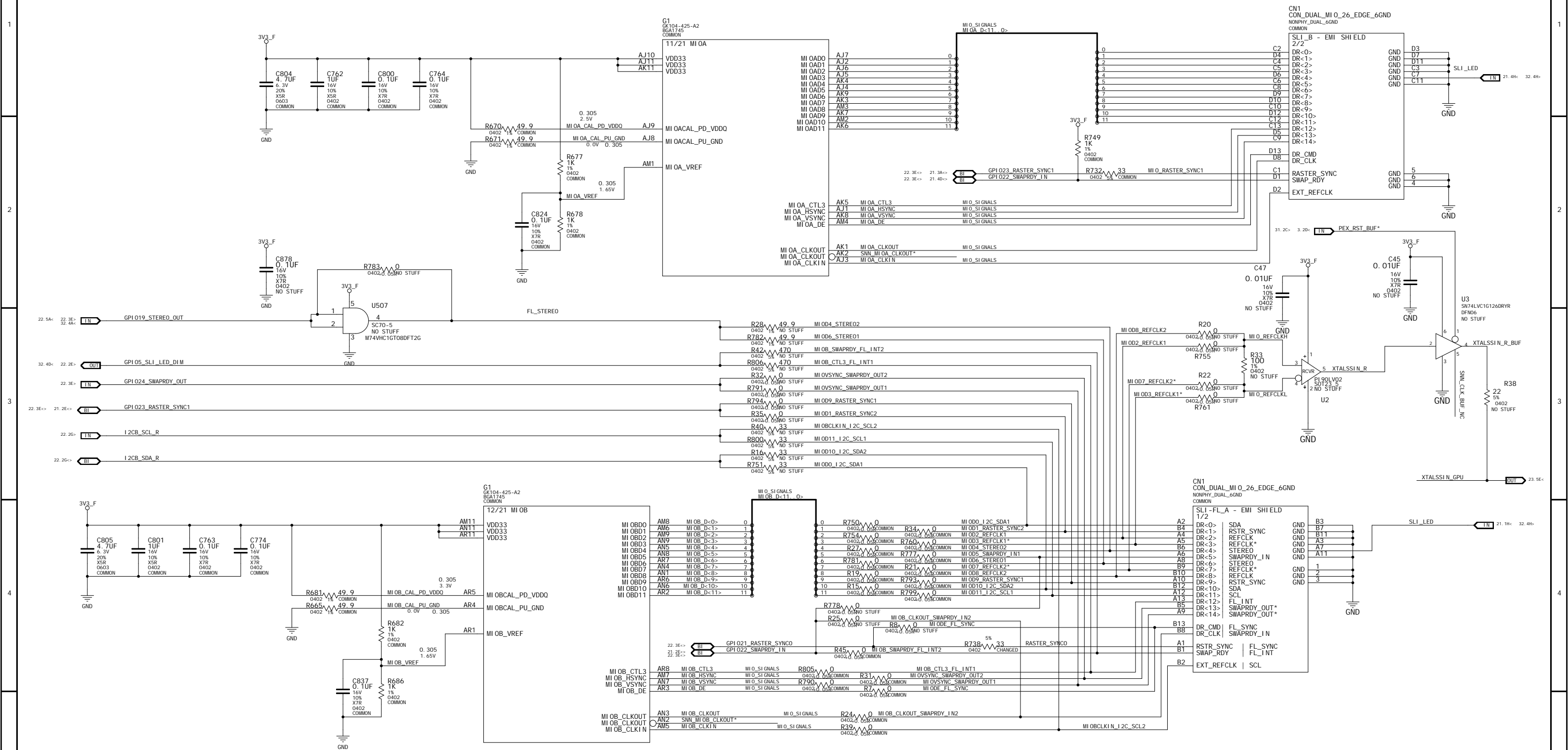


ASSEMBLY	SKU0000 GK104 256BIT 64Mx32
PAGE DETAIL	IFPD DP

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PCB REV	P2005-A01	PAGE	20 OF 33
BOM REV	B	DATE	26-MAR-2013

Page21: MI 0A/B Interface and FRAME LOCK



ASSEMBLY	SKU0000 GK104 256BIT 64Mx32
PAGE DETAIL	MI0A/B Interface and Frame Lock

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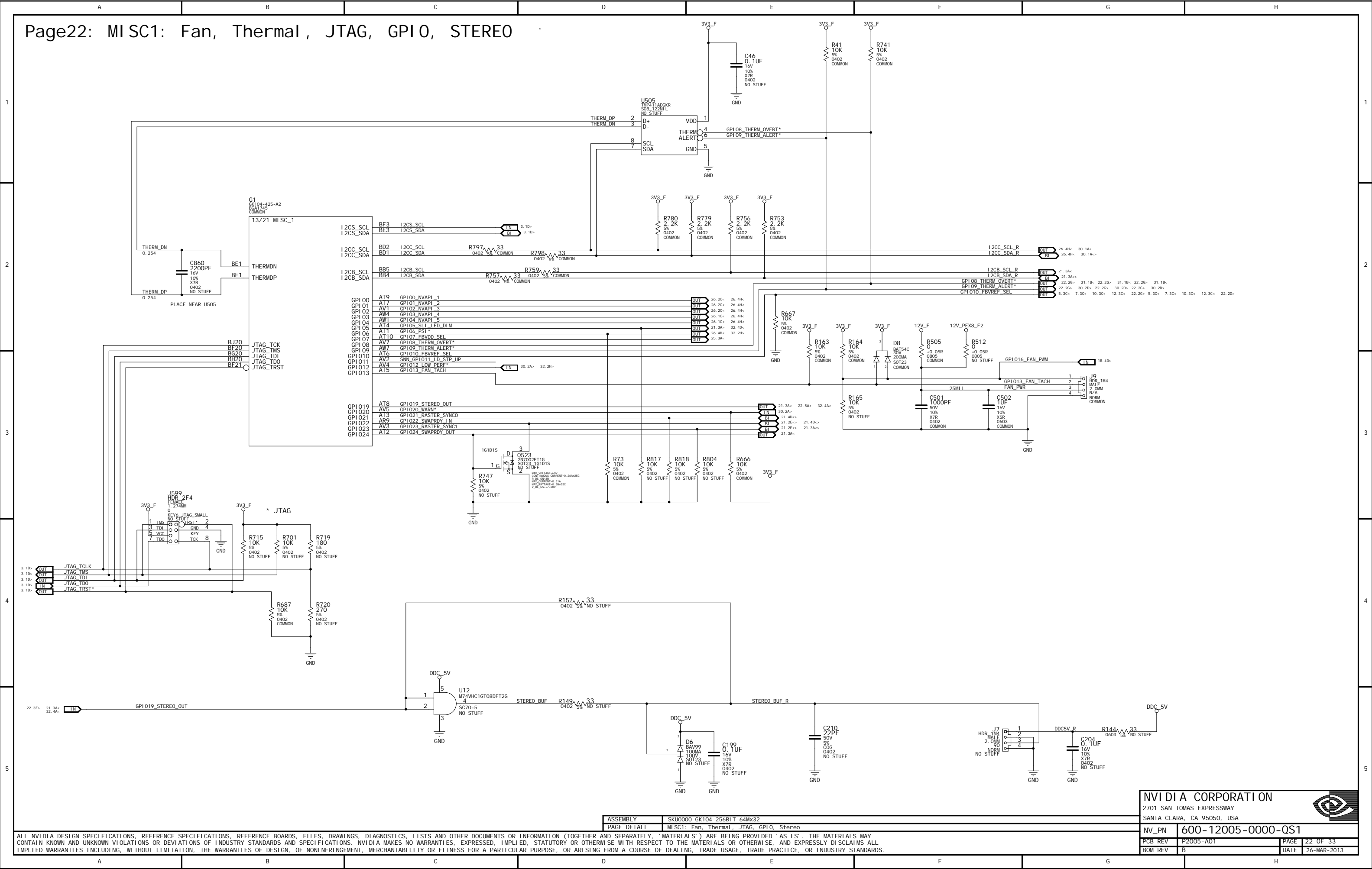
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PCB REV	P2005-A01	PAGE	21 OF 33
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BOM REV	B	DATE	26-MAR-2013
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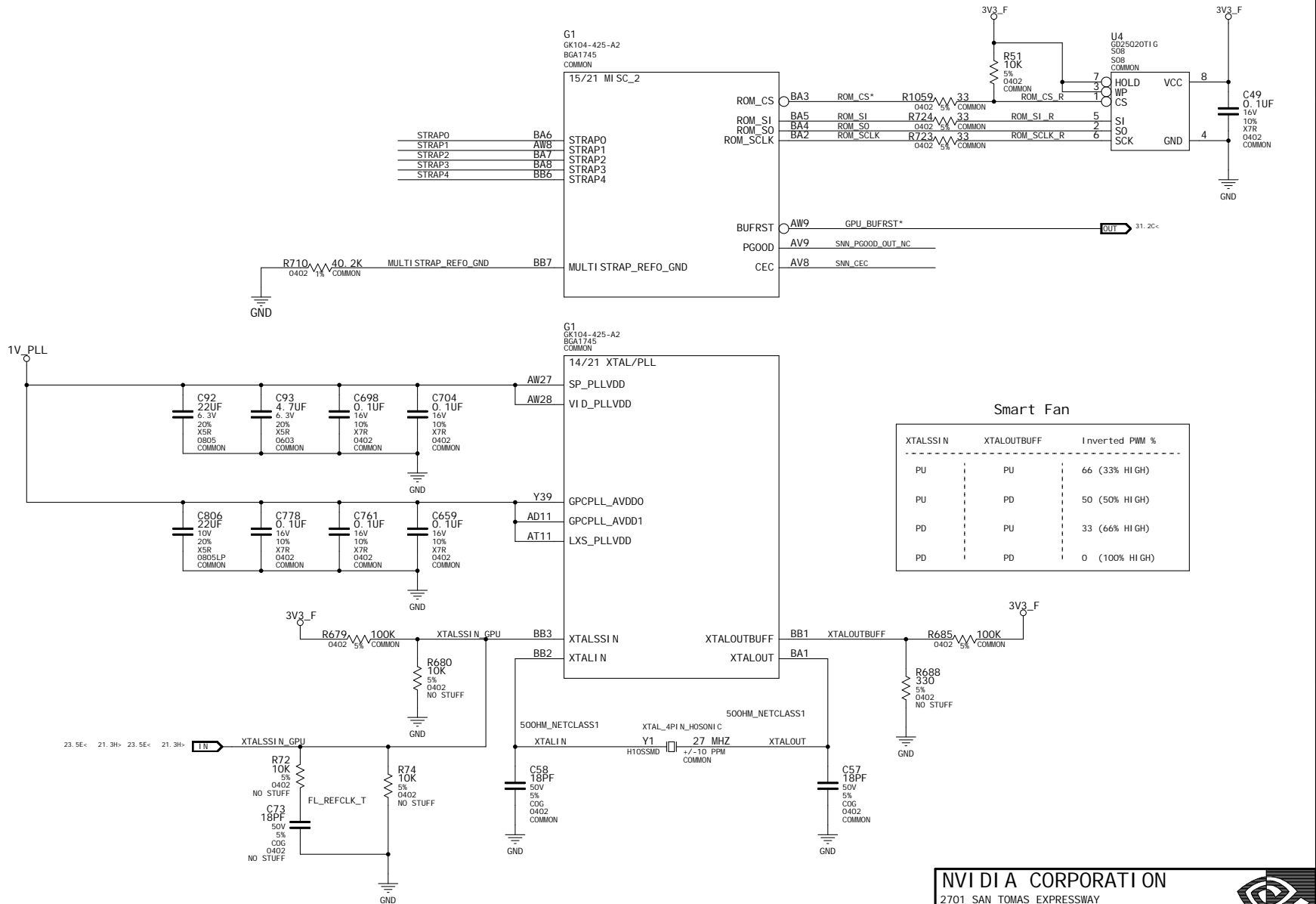
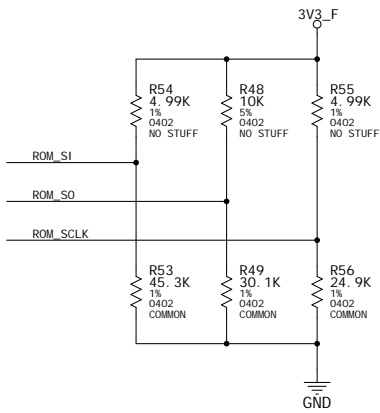
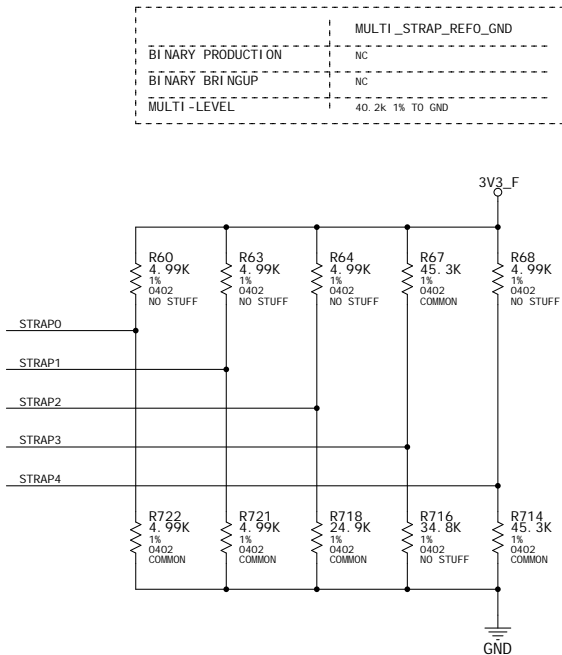
Page23: MI SC2: ROM, XTAL, Straps

STRAPO	USER_BIT [3:0]*	0000*	5K PD*
STRAP1	3GIO_PADCFG_LUT_ADR*	0000*	5K PD Desktop*
STRAP2	PCI_DEVID [3:0]*	0100 - (0x1184)*	25K PD -425 GPU*
STRAP3	SOR_EXPOSED [3:0]*	1111*	45K PU*
STRAP4	DP_PLL_VDD_33V*	1* FOR 3_3V*	
	PEX_MAX_SPEED*	1* FOR GEN2/3*	45K PD*
	PEX_SPD_CHANGE_GEN3*	1* ENABLED*	
	*		

	RAMCFG[0]*	1*	
ROM_SI	RAMCFG[1]*	1*	35K PD* 45K PD* 0110 for 64Mx32 256 bit HYNIX for SKU 0 primary memory 0111 for 64Mx32 256 bit SAMSUNG for SKU 0 primary memory
	RAMCFG[2]*	1*	
	RAMCFG[3]*	0*	
	VGA_DEVICE*	1*	
ROM_SO	SMB_ALT_ADDR*	0*	30k PD*
	FB[0]_APERTURE_SIZE*	1* For 128MB*	
	FB[1]_APERTURE_SIZE*	0* For 128MB*	
	PEX_PLL_EN_TERM100*	0* DISABLED*	
ROM_SCLK	PCI_DEVID_EXT[5]*	0* For 0x1184*	25K PD*
	SUB_VENDOR*	1* Dedicated BIOS*	
	PCI_DEVID_EXT[4]*	0* For 0x1184*	

	GND	3V3
5k	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111

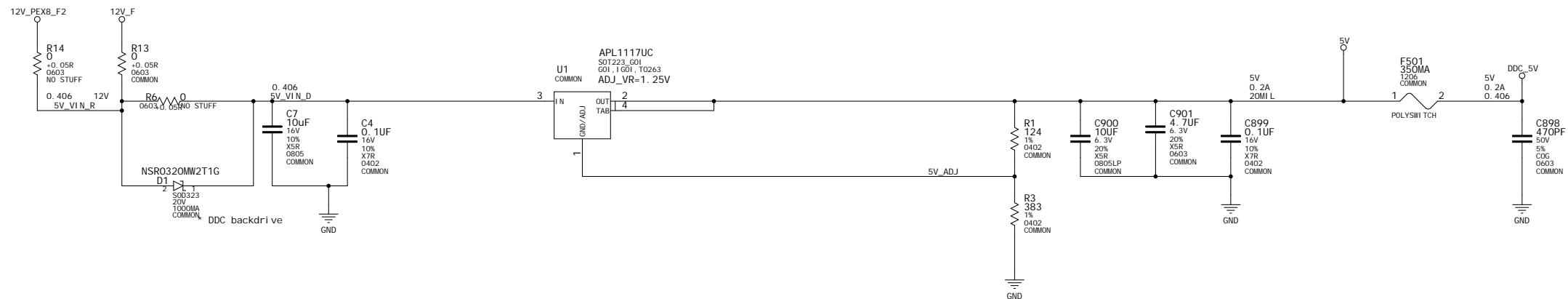
CFG[3:0]	Config Width	Vendor
0000	Reserved	
0001	32Mx32 256-bit Elpi da	
0010	32Mx32 256-bit Hyni x	
0011	32Mx32 256-bit Samsung	
0100	Reserved	
0101	64Mx32 256-bit Elpi da	
0110	64Mx32 256-bit Hyni x	
0111	64Mx32 256-bit Samsung	
1000	Reserved	
1001	32Mx32 192-bit Elpi da	
1010	32Mx32 192-bit Hyni x	
1011	32Mx32 192-bit Samsung	
1100	Reserved	
1101	64Mx32 192-bit Elpi da	
1110	64Mx32 192-bit Hyni x	
1111	64Mx32 192-bit Samsung	



Smart Fan		
XTALSSIN	XTALOUTBUFF	Inverted PWM %
PU	PU	66 (33% HIGH)
PU	PD	50 (50% HIGH)
PD	PU	33 (66% HIGH)
PD	PD	0 (100% HIGH)

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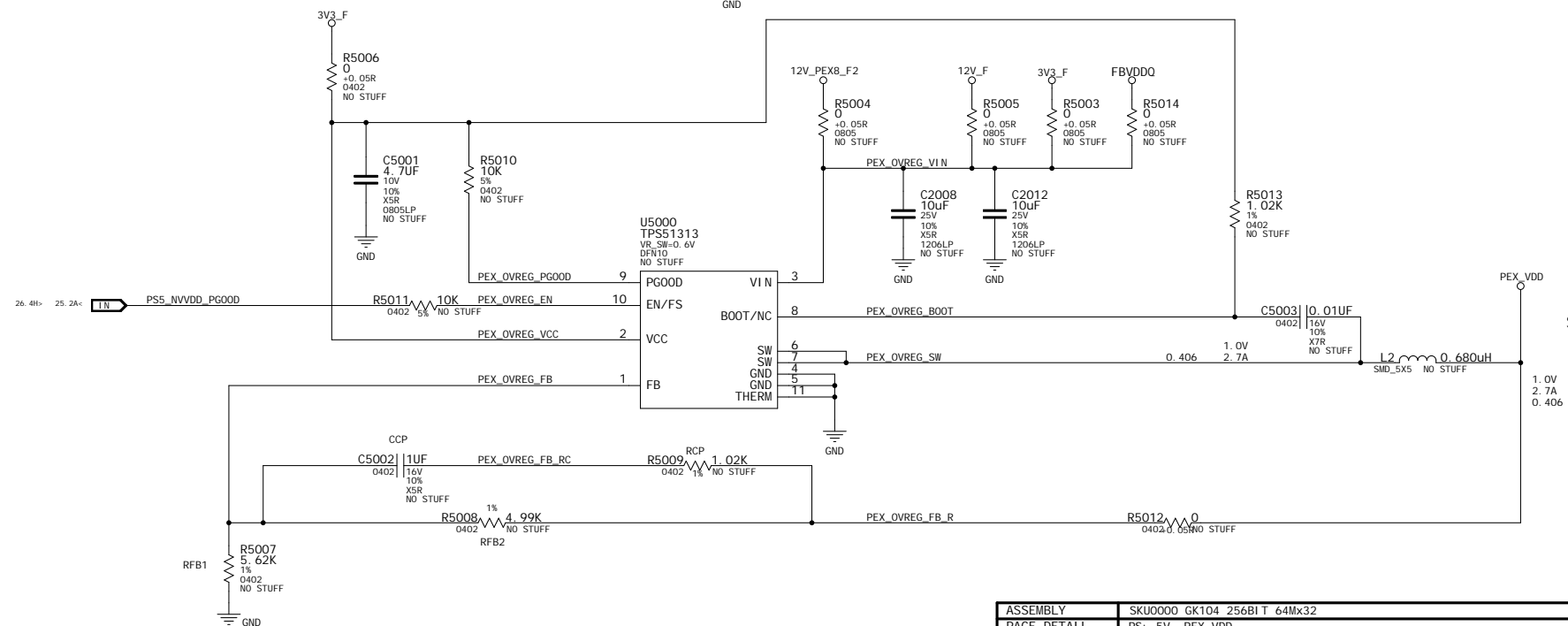
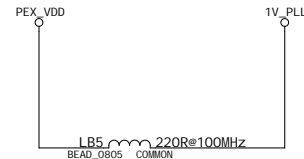
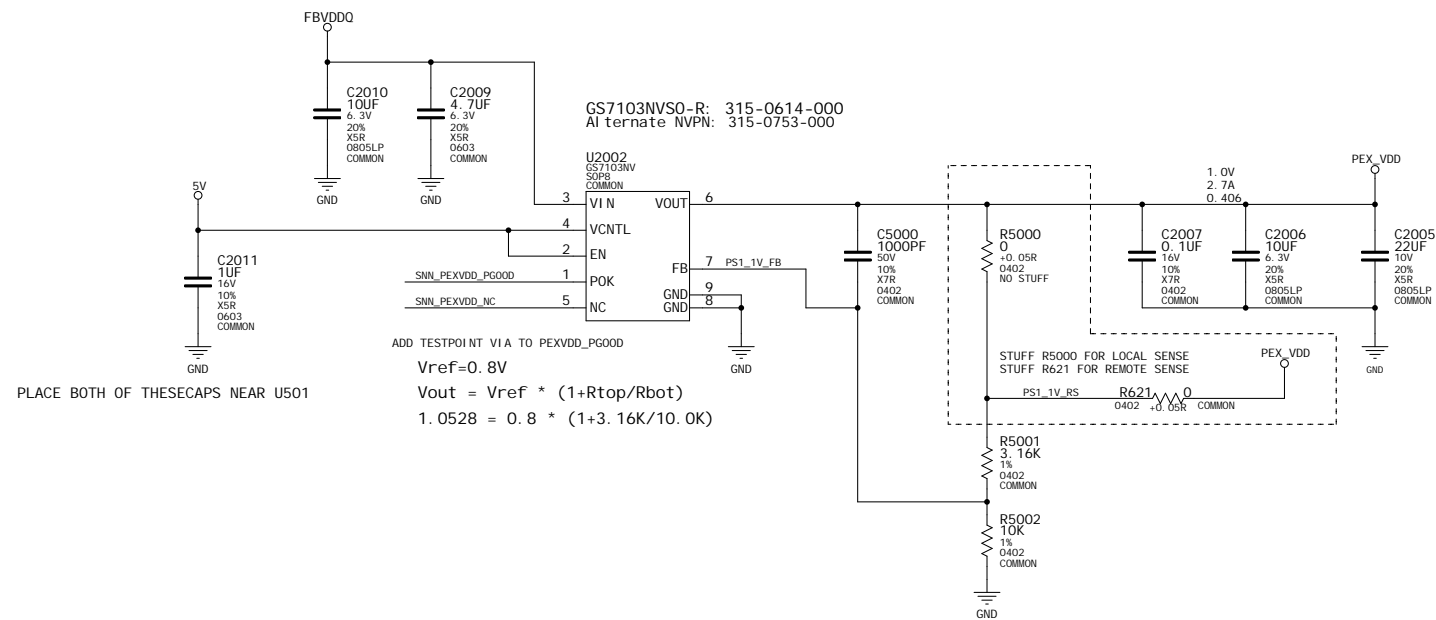
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NV_PN	600-12005-0000-QS1	
PCB REV	P2005-A01	PAGE 23 OF 33
BOM REV	B	DATE 26-MAR-2013



PEXVDD - PEX I/OVDD/Q


Vref=1.256V

$$V_{O_Typ} = 1.256 \cdot (1 + 383/124) + 60\mu A \cdot 383 = 5.16V$$

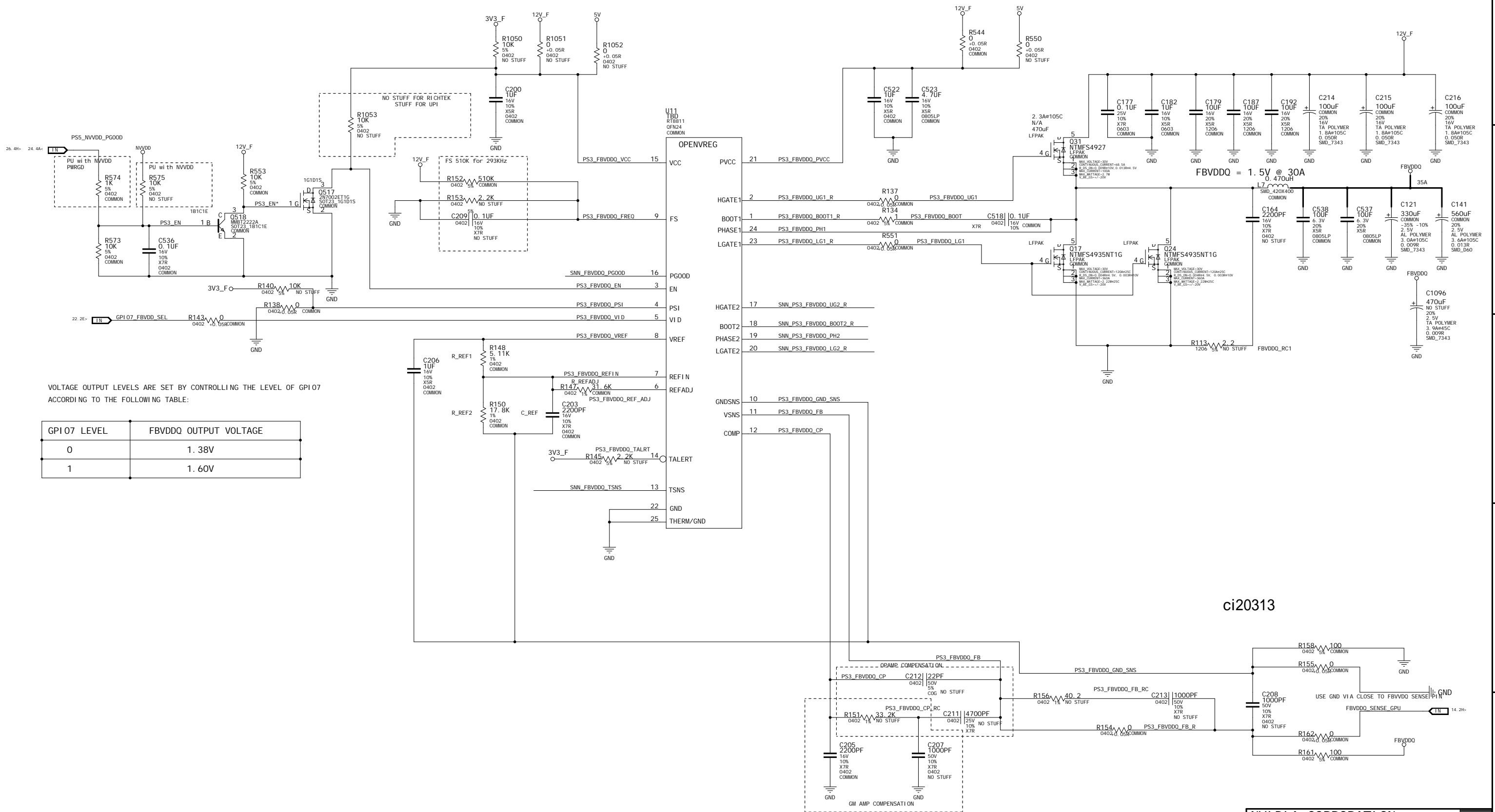


STUFF PEX_VDD OUTPUT CAPS ABOVE
WITH THIS REGULATOR

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PCB REV	P2005-A01	PAGE	24 OF 33
BOM REV	B	DATE	26-MAR-2013

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GPI 07 LEVEL	FBVDDQ OUTPUT VOLTAGE
0	1.38V
1	1.60V

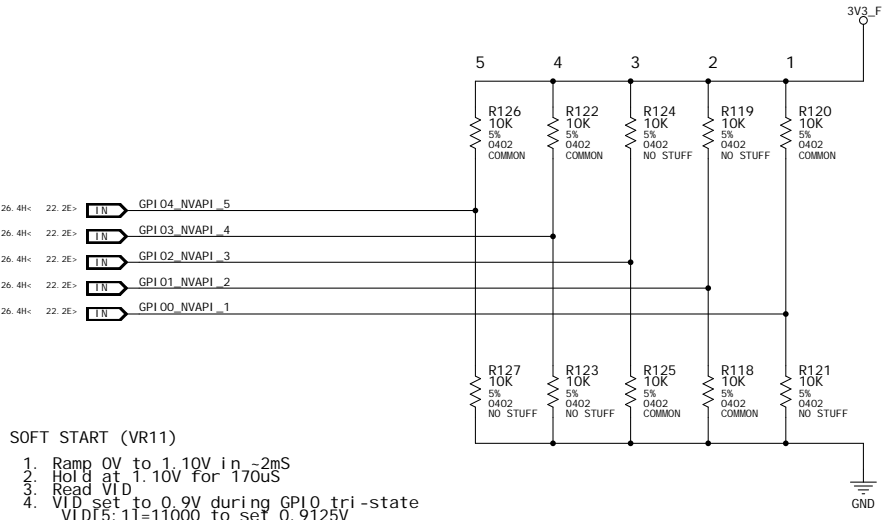
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ASSEMBLY	SKU0000 GK104 256BIT T 64Mx32
PAGE DETAIL	PS: FBVDD/Q

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PCB REV	P2005-A01	PAGE	25 OF 33
BOM REV	B	DATE	26-MAR-2013

VID Table					
GPI 04	GPI 03	GPI 02	GPI 01	GPI 00	VOUT
VID_5	VID_4	VID_3	VID_2	VID_1	
0	0	0	0	0	1.2125V
0	0	0	0	1	1.2000V
0	0	0	1	0	1.1875V
0	0	0	1	1	1.1750V
0	0	1	0	0	1.1625V
0	0	1	0	1	1.1500V
0	0	1	1	0	1.1375V
0	0	1	1	1	1.1250V
0	1	0	0	0	1.1125V
0	1	0	0	1	1.1000V
0	1	0	1	0	1.0875V
0	1	0	1	1	1.0750V
0	1	1	0	0	1.0625V
0	1	1	0	1	1.0500V
0	1	1	1	0	1.0375V
0	1	1	1	1	1.0250V
1	0	0	0	0	1.0125V
1	0	0	0	1	1.0000V
1	0	0	1	0	0.9875V
1	0	0	1	1	0.9750V
1	0	1	0	0	0.9625V
1	0	1	0	1	0.9500V
1	0	1	1	0	0.9375V
1	0	1	1	1	0.9250V
1	1	0	0	0	0.9125V
1	1	0	0	1	0.9000V
1	1	0	1	0	0.8875V
1	1	0	1	1	0.8750V
1	1	1	0	0	0.8625V
1	1	1	0	1	0.8500V
1	1	1	1	0	0.8375V
1	1	1	1	1	0.8250V



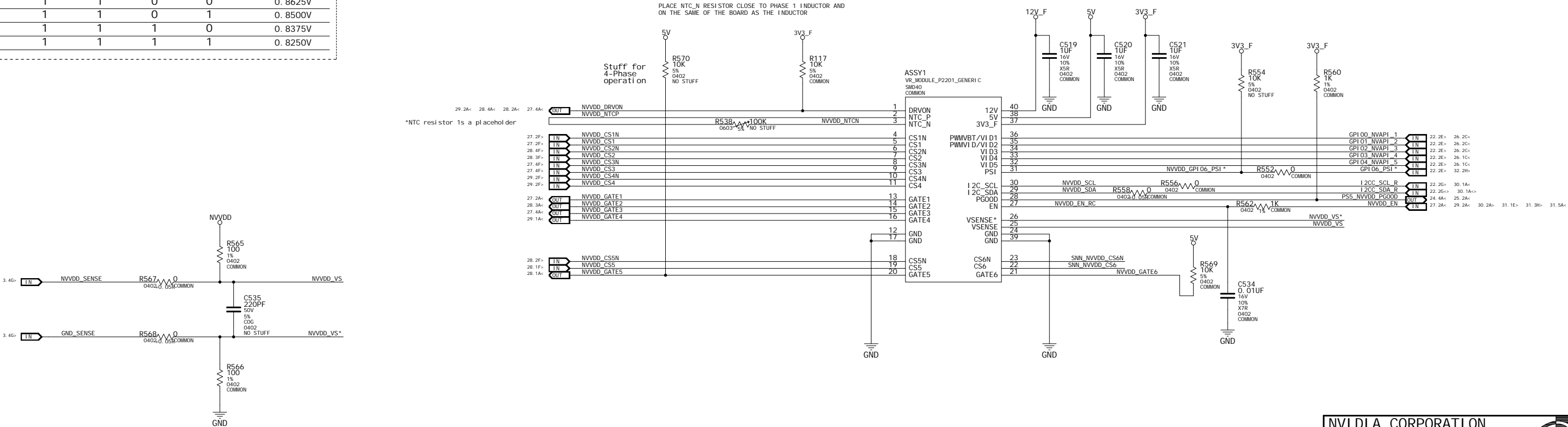
SOFT START (VR11)

1. Ramp 0V to 1.10V in ~2ms
2. Hold at 1.10V for 170us
3. Read VID
4. VID set to 0.9V during GPI 0 tri-state
VID[5:1]=11000 to set 0.9125V

P-STATE VOLTAGES

1. P0 at 1.05V to 1.15V (depending on VB)
2. P8/P12 at 0.80V

PSI intended for lower power states
switching from 5 phases down to 1 or 2 phases
PSI DRVON enabled for either 3 or 4 phases

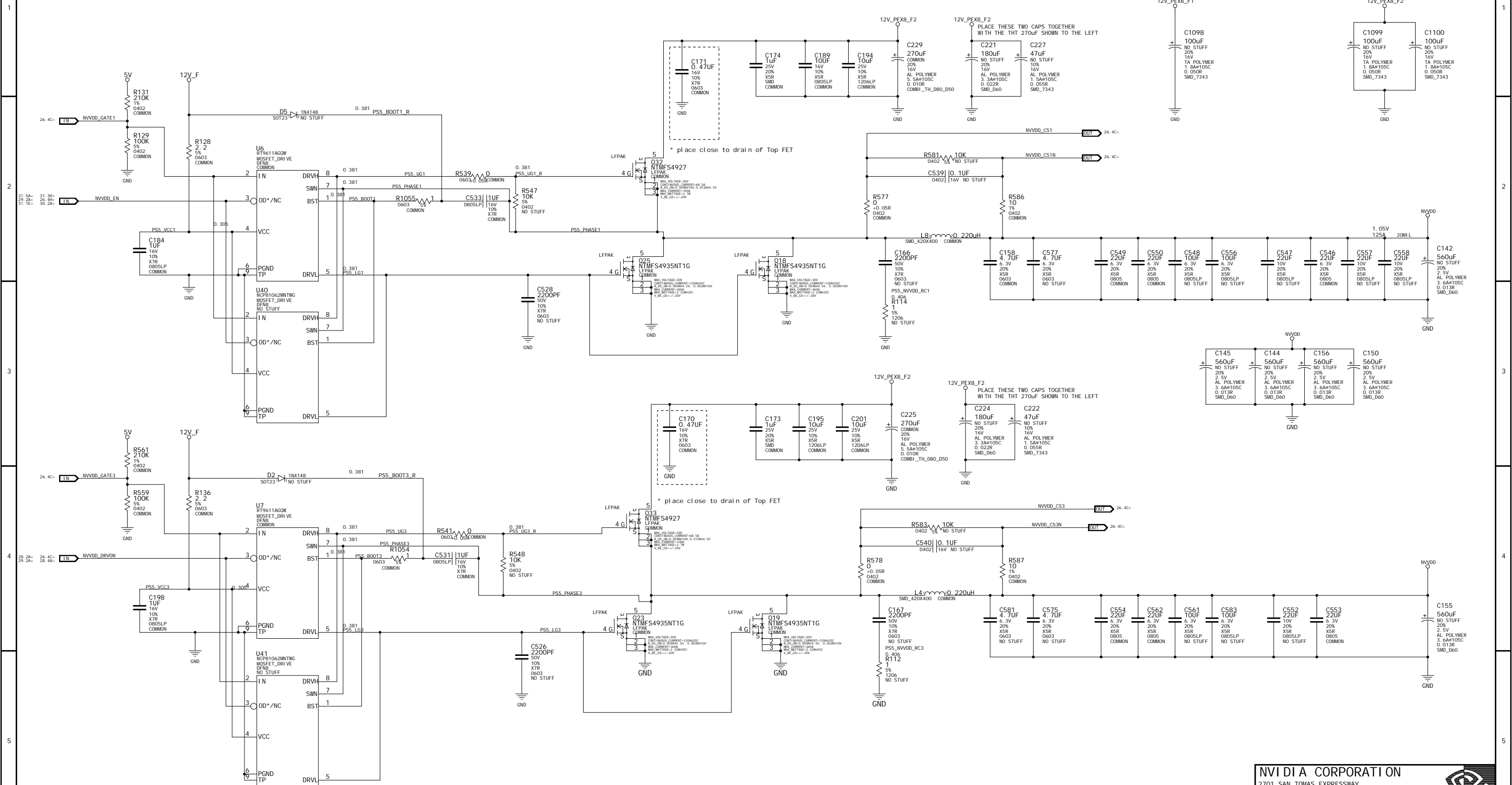


*NTC resistor is a placeholder

Page27: PS: NVVDD Phase 1, 3

PLACE ONE OF THESE NEAR TOP FET OF PH1 or PH3

PLACE ONE OF THESE NEAR TOP FET OF PH5



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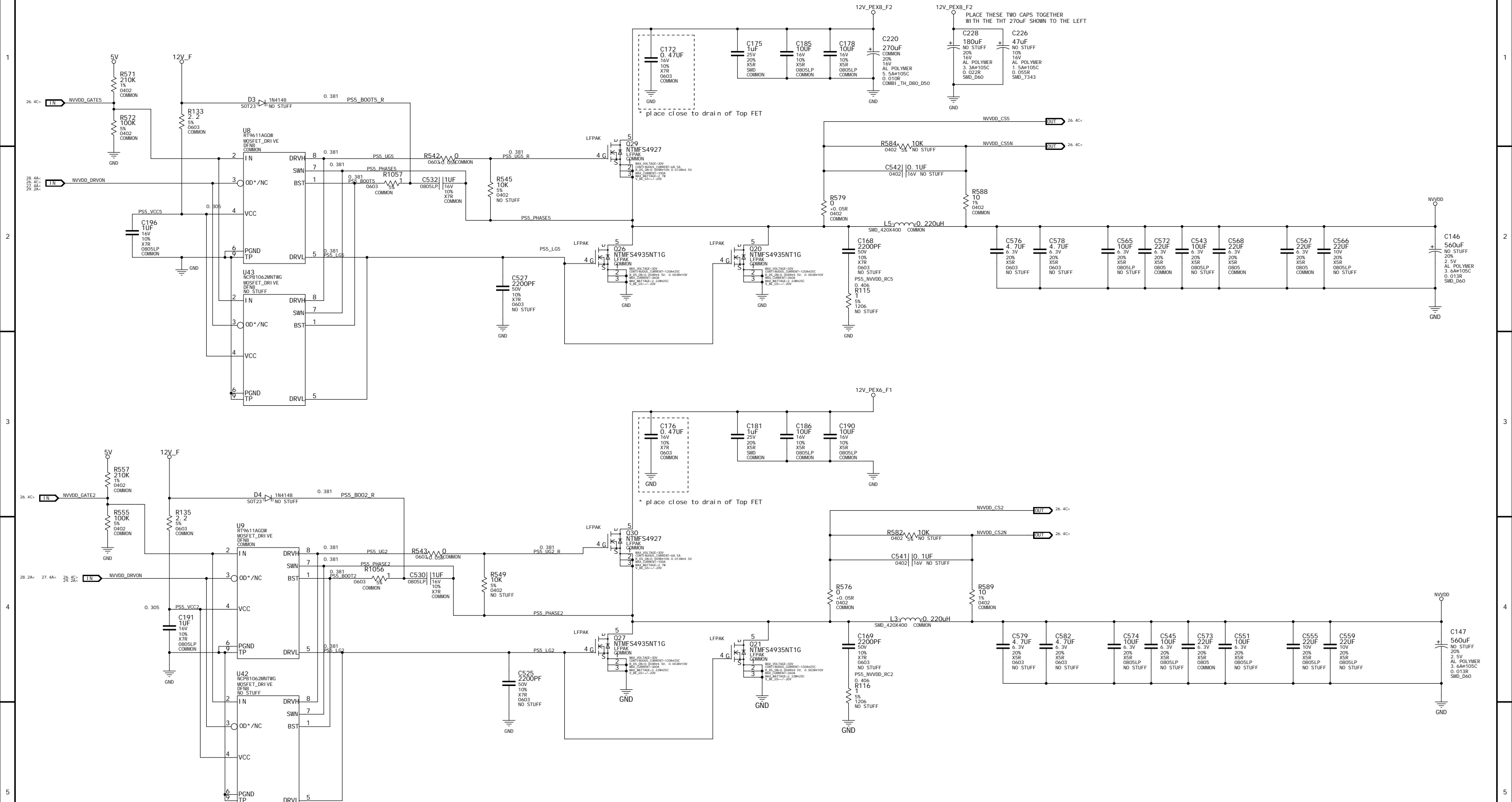
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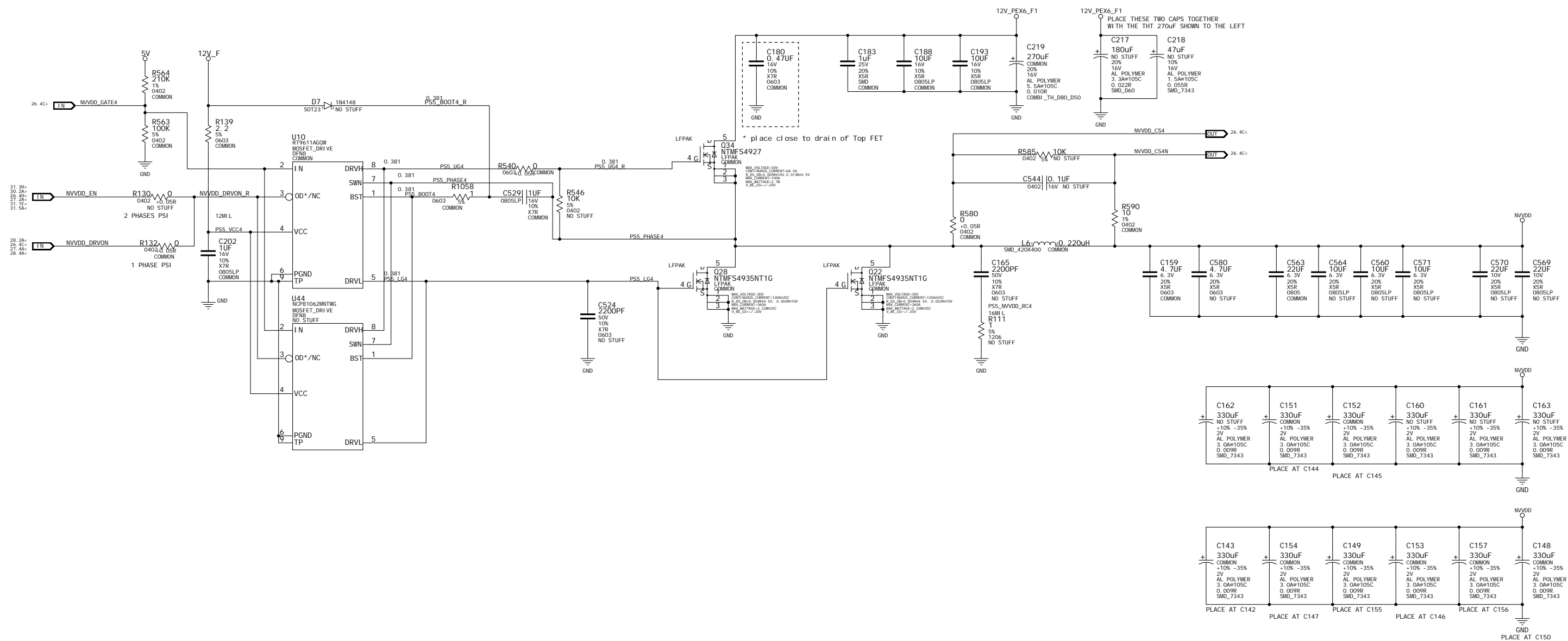
NV_PN	600-12005-0000-QS1
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PCB REV	P2005-A01	PAGE	27 OF 33
BOM REV	B	DATE	26-MAR-2013

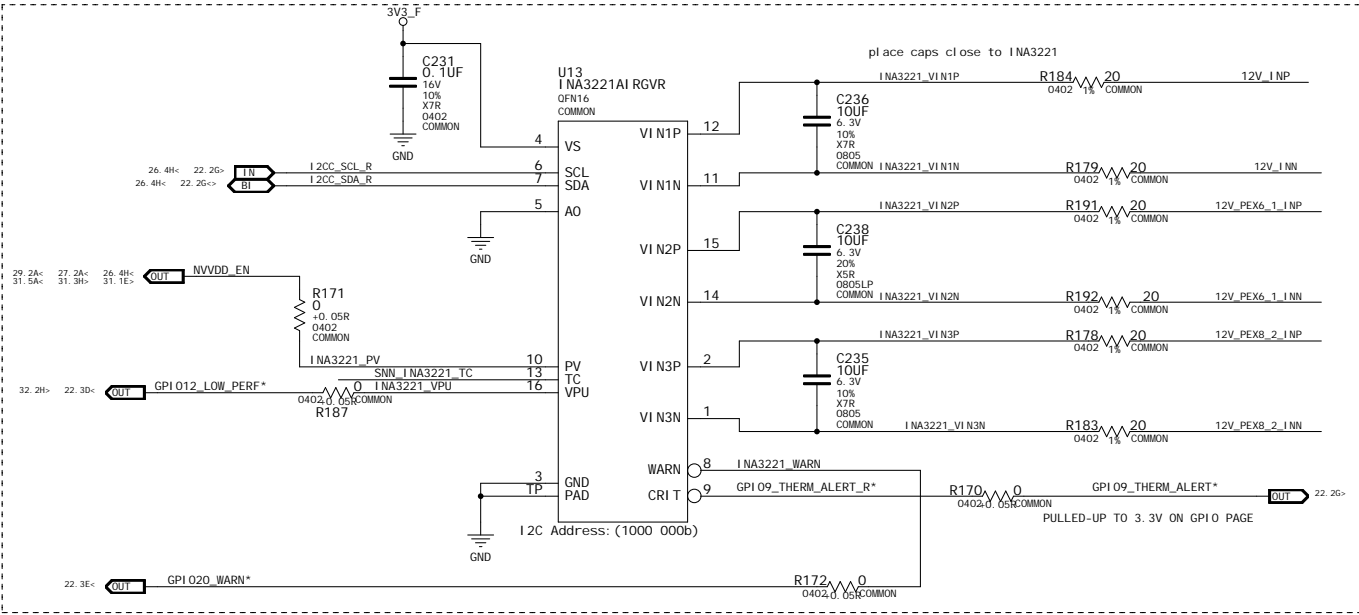
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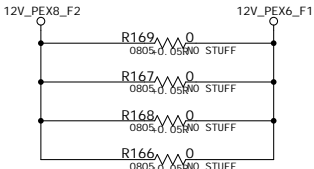
Page30: PS: Inputs, Filtering, and Monitoring



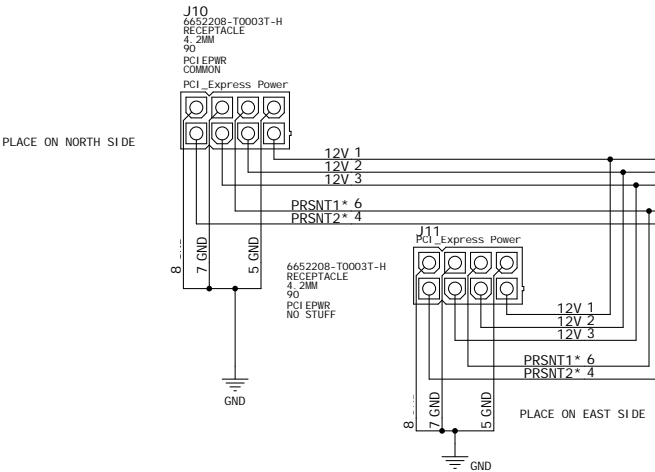
PEX6 INPUT 1 - 2x3 PCIE CON 75W



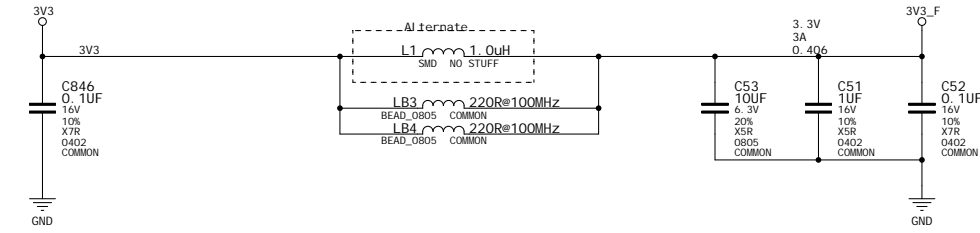
STUFF BOTH FOR QUADRO
PLACE NEAR U502 (INA3221)



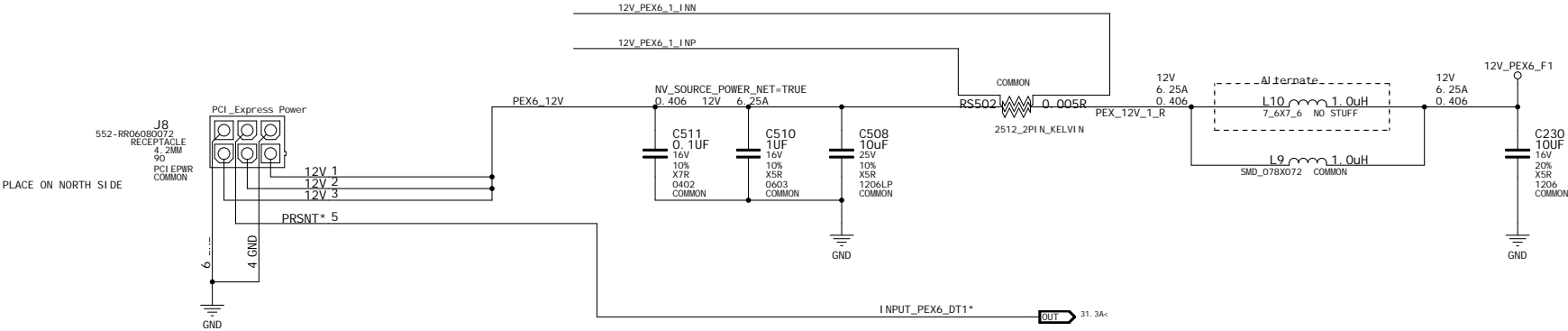
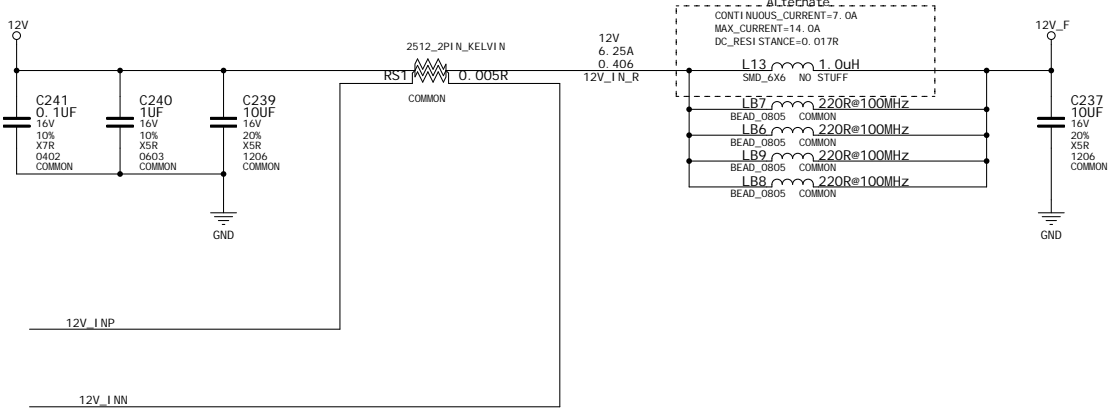
STUFF ALL FOUR FOR QUADRO



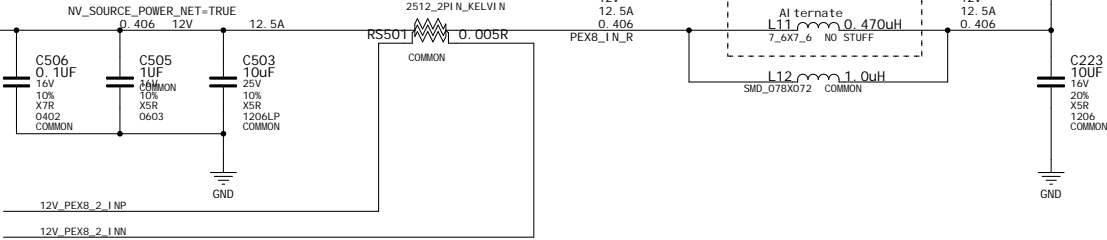
PEX 3V3 INPUT - 10W



PEX_12V INPUT - 66W



PEX8 INPUT 2 - 2x4 PCIE CON 150W



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NV_PN	600-12005-0000-QS1		
PCB REV	P2005-A01	PAGE	30 OF 33
BOM REV	B	DATE	26-MAR-2013

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THERM OVERT SHUTDOWN LATCH

I FP_I OVDD (backdri ve preventi on)

PEX Input - NVVDD Power Sequence

PEX Input Present 1

PEX Input Present 2

POWER CONNECTOR HOT-UNPLUG DETECT

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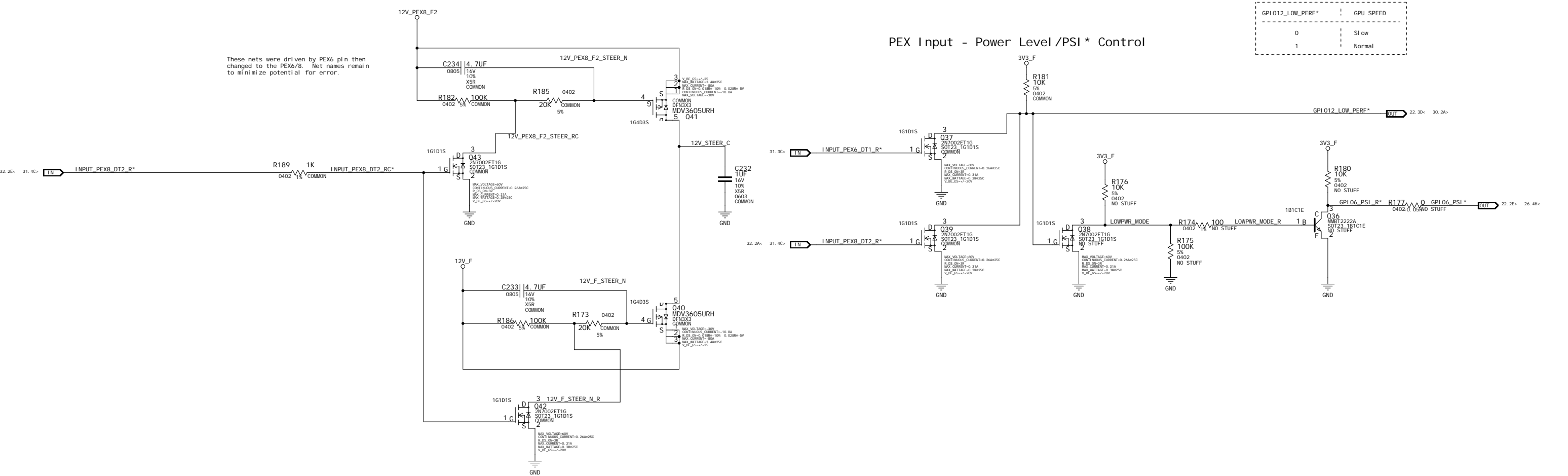
PCB REV	P2005-A01	PAGE	31 OF 33
BOM REV	B	DATE	26-MAR-2013

PEX Input - 12V Current Steering FETs

These nets were driven by PEX6 pin then changed to the PEX6/8. Net names remain to minimize potential for error.

PEX Input - Power Level /PSI * Control

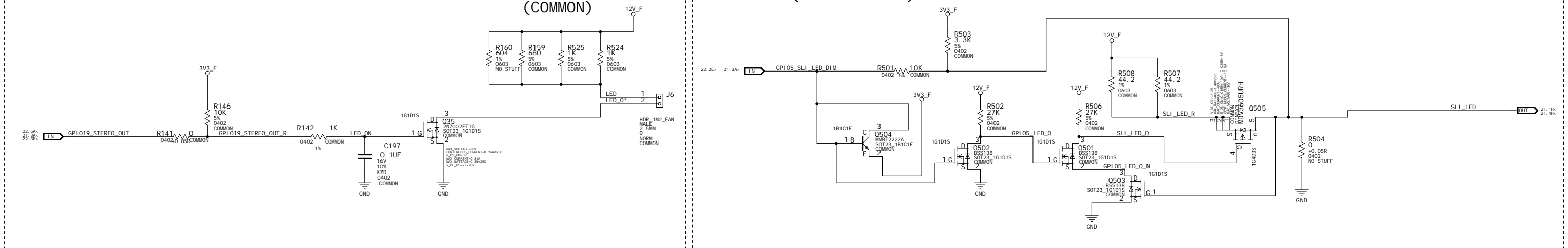
GPI012_LOW_PERF*	GPU SPEED
0	Sl ow
1	Normal



GeForce Logo LED

LED HEADER (COMMON)

SLI LED (GEFORCE ONLY)



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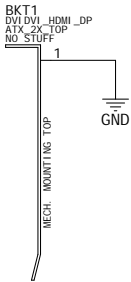


ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: 12V Current Steering PSI Control and LED

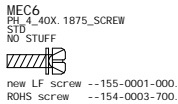
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PCB REV	P2005-A01
BOM REV	A
PAGE	32 OF 33
DATE	26-MAR-2013

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Brackets:



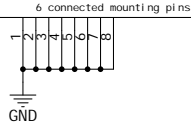
Bracket Screw



Hockey Stick

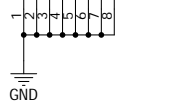


BGA SOCKET ASSY

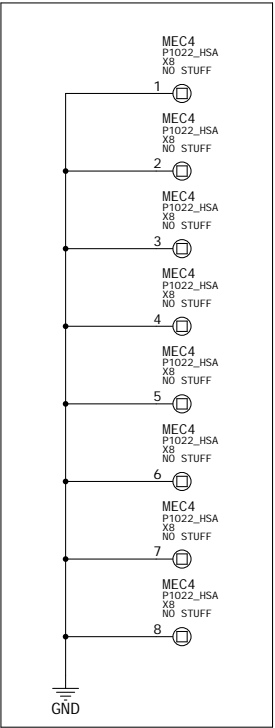
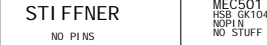


GPU Sti ffner

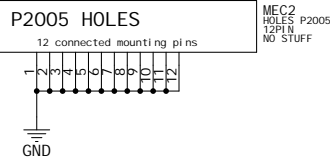
BOARD STIFFENER



STIFFNER



Mechani cal Hol es Symbol



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PCB REV P2005-A01 PAGE 33 OF 33
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